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DEMONSTRATION OF PULSED ELECTRON BEAM APPLICATIONS (PEBA) FOR FABRICATING SMALL GEOMETRY SEMICONDUCTOR DEVICES

ANTON GREENWALD
(617) 275-6000

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This is the final report of a program demonstrating the applicability of pulsed electron beam processing to the fabrication of small-geometry silicon semiconductor devices, with the concomitant elimination of the high-temperature thermal treatments that can degrade performance. The report documents the use of pulsed annealing techniques to fabricate diodes, ion-implanted resistors, and transistors with electrical characteristics comparable to devices fabricated by high temperature thermal processing.

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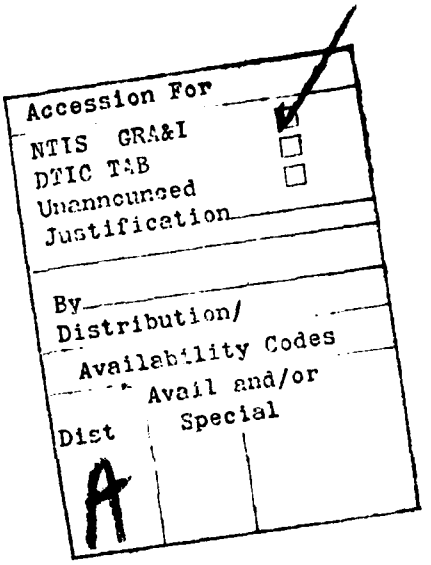
Pulsed liquid phase epitaxial regrowth of polysilicon films were demonstrated. Resolution with oxide masks to one micron has been shown to be feasible.



SUMMARY

The objective of this program was to demonstrate the advantages of pulsed electron beam processing in the fabrication of silicon integrated circuits. The use of pulsed surface heating permits lower temperatures to be maintained, reducing plastic deformation and distortion of the substrate, unwanted diffusion from buried layers, and the formation of defects and precipitates. Lower temperatures can be expected to increase the yield for very small line-width devices.

The specific processes studied in this program are the formation of epitaxial silicon on silicon layers and the annealing of ion implantation damage by pulsed electron beams. Both processes now require typical temperatures in excess of 900°C. Results show that the use of a pulsed electron beam to replace high temperature furnace cycles allows the reduction of processing temperatures below 600°C. Specifically, it has been demonstrated that:

- Polysilicon films deposited on single-crystal substrates at 600°C by LPCVD can be regrown epitaxially by pulsed electron beam liquid phase epitaxy.
- Arsenic, boron, and phosphorus ion implants in the energy range 10-100 keV for dose levels 10^{13}-10^{16} ions/cm^2 can be annealed by pulsed electron beam processing.
- Implanted resistors, diodes, and transistors with good electrical characteristics can be fabricated by pulsed electron beam annealing.
- Oxide masks can be used to define pulsed electron beam process areas to better than one micron resolution.

The feasibility of using pulsed electron beam processing for the fabrication of VLSI devices has been demonstrated.

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TABLE OF CONTENTS

TABLE OF CONTENTS (Concluded)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Concluded)

LIST OF TABLES

SECTION 1
INTRODUCTION

1.1 PROGRAM OBJECTIVES

The goal of this program was to demonstrate that large area pulsed electron beams can be used to reduce the maximum temperature used in processing large-scale integrated circuits. Specific processes studied were the annealing of ion implantation damage and the deposition of epitaxial silicon layers. Small geometry diodes and transistors were successfully fabricated to demonstrate the utility of pulsed electron beam applications (PEBA).

1.2 TECHNICAL APPROACH

Existing technology for the fabrication of integrated circuits uses temperatures exceeding 800°C for the deposition of epitaxial films[1] and for annealing of ion implantation damage.[2] Plastic deformation of the substrate and diffusion from previously deposited layers can occur at these temperatures which limit submicron dimension device performance.[3] This program has demonstrated that epitaxial thin films can be formed, and that active implanted device junctions can be fabricated by PEBA, without heating the substrate to high temperatures. This approach restricts the motion of the dopant, generates fewer dislocations, and results in lower contamination for both process steps.

High-temperature furnace processing steps were replaced by pulsed electron beam surface heating.[4] Through control of fluence and particle energy, electron beams were used to heat silicon to a depth of one micron, allowing temperature in the bulk of the wafer to rise no more than 10°C. Brief thermal gradients caused epitaxial crystal growth in the heated surface material to anneal ion implantation damage, and to recrystallize low temperature deposited polycrystalline or amorphous silicon films. By using a low temperature deposition technique (LPCVD) followed by PEBA, lightly doped high-quality epitaxial films over a heavily doped substrate have been formed. Based upon a multiple-step low-temperature furnace and low-fluence pulsed electron beam treatment, a process was developed to anneal ion-implanted junctions for small-scale devices. This process showed excellent activation with minimal lateral diffusion of the dopant.

1.3 TECHNICAL RESULTS

1.3.1 Process Achievements

The major program goals have been achieved in that the utility of PEBA for (i) the formation of epitaxial layers and (ii) annealing junctions at low temperatures has been demonstrated. Specifically, the program has demonstrated that:

(i) Arsenic, boron and phosphorus ion implants at doses over 10^{13} ions/cm^2 to depths as deep as 0.5 micron can be annealed.

(ii) PEBA (with melting) produces electrical results as good as furnace anneals while restricting the lateral and vertical motion of a junction to less than 0.25 micron.

(iii) PEBA can be used for annealing a shallow ion-implant without affecting (diffusing) a deeper (1 micron) junction; however, junctions can be driven deeper by appropriate choice of fluence.

(iv) PEBA processing is compatible with patterns defined by oxide films when over 0.3 micron thick.

1.3.2 Device Demonstrations

As part of the demonstration requirements for this program, the following devices were fabricated using PEBA:

- Ion-implanted (low dose) resistors
- Low leakage current n+p and p+n diodes
- Bipolar transistors
- JFETs

Device fabrication can be divided into two groups: large devices fashioned for electrical measurements and small devices used to test geometrical limitations. The small devices, using line widths as narrow as 1 micron, are discussed in Section 2.5. They consisted of (1) a set of ion-implanted resistors formed in oxide windows of varying thickness (from 1.3 to 50 microns wide), (2) a parallel line pattern etched in oxide (2.5 micron fingers spaced 3.5 micron apart), and (3) a repeat of the second test with 1-micron fingers spaced 2 microns apart. There was no variation of sheet resistance for the resistor pattern and the other tests gave the 0.2 micron upper limit for lateral diffusion of a junction.

The large devices included an extended series of diodes (0.02 to 0.5 mm diameter) discussed in Section 2.6. All PEBA diodes had low-leakage current, good ideality factors, and high lifetime if a post-pulse anneal of 550°C was included in the process sequence. Activation of the implanted dopant was comparable to thermal anneals; however, the minority carrier lifetime was a factor-of-two lower for PEBA. Analysis by electron beam induced current (EBIC) showed that there are some defects after PEBA below the junction but not deeper than one micron. Previous DLTS measurements [5] imply that most of these defects are annealed after a post-PEBA thermal cycle at 550°C.

More complex devices, discussed in Section 2.7, were fabricated by PEBA of shallow ion-implanted junctions placed over deeper junctions. A bipolar transistor with a gain of 40 was similar to a thermally annealed implanted transistor. A series of JFET's was successfully fabricated in an n-type, one micron thick CVD epitaxial layer on a p-type substrate. I-V characteristics were obtained for low- and high-fluence pulse anneals with equal parameters for a furnace anneal. In this case, both low and high dose, boron and phosophorus implants were annealed simultaneously. JFET leakage current was low. An unsuccessful attempt was made to fabricate a JFET in a PEBA epitaxial layer. This second process requires more development; however, Schottky-barrier diodes (Section 3.5) were successfully fabricated in this material.

SECTION 2
LOW TEMPERATURE JUNCTION FORMATION

2.1 DEFINITION OF REQUIREMENT

The objective of this part of the program was to demonstrate the feasibility of annealing patterned ion-implanted junctions using PEBA. A second objective was to demonstrate annealing by PEBA for a variety of implant parameters, not previously tested, but encountered in integrated circuit technology.

The deleterious effects associated with high-temperature ion-implant annealing are wafer warpage, dopant diffusion, and contamination. Dopant diffusion and the implied lateral junction motion are critical for submicron design rules, as two implanted regions are very likely to be separated by the minimum linewidth (for the gate) in an integrated circuit. Contamination problems from a furnace are more severe for very small devices where the defect density must be reduced. Low-temperature processing reduces diffusion of dopants, reduces contaminants, and prevents wafer warpage. However, low temperature annealing in a furnace does not fully remove radiation damage or fully activate the dopant in room temperature ion implants.[6] For reference purposes in this discussion a temperature above 700°C can be considered high, since further processing after annealing, such as oxide growth, will require temperatures about this level but no higher.

The approach to low-temperature processing in this program is to use pulse electron beam applications (PEBA) technology to replace high temperature thermal steps where desired. Two pulsed techniques are available - liquid and solid phase epitaxy. Liquid phase epitaxy uses the electron beam to melt the silicon to some desired depth, below the implant, and restores perfect crystal structure upon cooling.[4] Solid phase epitaxy is a two step anneal, with a low temperature thermal treatment (e.g., 550°C for 2 hours) restoring the crystal structure,[7] and a pulse at non-melting fluence levels activating the dopant. Each process has different applications.

All of the advantages of low temperature processing were realized by PEBA. In addition, the liquid phase epitaxy technique was shown to reduce dislocation density in the annealed, implanted regions compared to furnace processing.[4] PEBA affected only the near surface region, and did not diffuse junctions below the implants, about 1 micron

deep. Masking of the PEBA process was easily accomplished with the oxide used to mask ion implantation. Even with the high fluence pulse a thin layer of SiO_2 was sufficient to absorb most of the electron beam energy, without retaining the charge, so that the silicon below the oxide did not melt. There were no oxide-edge effects. This compares favorably with pulsed laser annealing where the oxide does not act as a mask, and interference effects at a beveled oxide edge caused damage to annealed silicon.

2.2 PULSED ELECTRON BEAM SOURCE

2.2.1 Operation

The experiments performed for this program used the SPI-PULSE^{TM} 6000 pulsed electron beam generator.[4] This equipment is similar to flash x-ray sources, and does not work like an electron microscope or similar equipment with continuous beams. Energy is stored on a high-voltage transmission line which acts as a capacitor and is charged by a d.c. power supply. When triggered, the transmission line provides a short (80-100 ns) fast risetime electrical pulse to the diode. The diode consists of a large-diameter high-purity graphite cathode and a fine-mesh tungsten anode. The electron beam is emitted from a carbon plasma which forms at the cathode when a very high voltage is applied.[8] With proper choice of parameters, the peak diode current corresponds to a low diode voltage, which results in a flat electron energy spectrum with a typical average particle energy of 12 keV (see ref. 4).

The sample wafer is held just behind the anode at a varying distance of 5 to 25 mm. This distance, and the strength of an applied magnetic field, is adjusted to vary the diameter of the electron beam at the sample, the uniformity of the beam, and the angle of incidence for electrons impinging upon the sample. Electron beam diameter is typically 20 to 75 mm at the sample with an angle of incidence between 30 and 60 degrees. Samples are mounted in a shallow depression in a holder, face-up horizontally with no clamps or other materials covering the area irradiated by the beam. Samples can be mounted in a thermally isolated but electrically grounded holder and radiantly heated to 400°C just before pulsing. For most work, however, the sample remains at room temperature.

2.2.2 Beam Interactions

Self electric and magnetic fields of the electron beam used in these experiments dominate propagation and sample interaction mechanisms. Typical beam parameters are 20 kA in a 5 cm diameter at 12 kV. Peak resulting magnetic fields due to this current are over 1 kG. Electric fields, which vary with the geometry of the conducting surfaces, exceed 50 kV/cm. Close spacing betwen the conductive planes of the cathode, anode, and sample reduce radial electric fields. Electron motion, dominated by magnetic fields, is to focus inward or to pinch the beam envelope. This focusing action is controlled by applying an axial magnetic field, which causes the beam to rotate. Focusing the beam onto the sample; (1) reduces the fluence at the anode relative to that at the sample (so the anode does not melt), (2) increases electrostatic interaction between the electrons in the beam which improves uniformity and reduces shadowing from the anode mesh, and (3) causes the electrons to impinge upon the wafer at high angles of incidence. Non-uniform interactions between the beam and the wafer are avoided by providing a low inductance, low resistance ground return for the high current.

2.2.3 Beam Characteristics

The uniformity of processing by an electron beam is better than $\pm$10 percent, and is expected to be improved.[9,10] The key beam parameter is the fluence, or energy per unit area incident upon the wafer, which determines the maximum surface temperature and/or melt depth. For silicon, typical values are between 0.8 to 1.4 J/cm^2. When the uniformity was measured directly with an array of calorimeters, which averaged the fluence over an area of approximately 1 cm^2, the results varied no more than $\pm$4 percent. To measure the processing effect, a 75 mm wafer was implanted with 5×10^{15} ions/cm^2 of arsenic at 25 keV. After annealing by PEBA the sheet resistance varied $\pm$10 percent across the entire surface.[9] The variation changes with the process. PEBA of polycrystalline silicon films was uniform to $\pm$7 percent on a microscopic scale.[10]

The reproducibility of this equipment is better than $\pm$1 percent. In typical tests the diode voltage and current traces displayed on an oscilloscope[8] will overlap perfectly. In tests for JPL, 500 implanted wafers were successfully processed by PEBA.[9]

The measured carbon contamination from the cathode plasma is less than 10^{12} atoms/cm^2 at the sample.[9] In a clean PEBA processing system, the carbon concentration of the sample was not detectable.[5] Contamination from the anode was also undetectable, except when the anode began to melt at fluence levels above normal processing requirements.

2.3 MODEL OF PULSED ELECTRON BEAM ANNEALING

2.3.1 Overview

A large-area pulsed electron beam can be used to anneal the implantation damaged surface of a single crystal silicon wafer. Figure 1 presents a model of the near surface temperature profiles after a sample is irradiated by a very brief pulse of energy which is absorbed in a shallow layer. Thermal diffusion during this pulse is small, so that the thermal energy is confined to the near-surface region. Typically, the pulsed beam melts the silicon wafer to a depth of 0.5 micron. This molten layer cools rapidly by thermal conduction into the thick substrate (quenching), causing the liquid-solid interface to move toward the surface at velocities exceeding 0.5 m/s. Crystal structure is restored by liquid phase epitaxy at the liquid-solid interface.

An elaboration of this model is given in the remainder of this subsection. Calculations of electron energy deposition and thermal profiles are presented. A discussion of thermal properties of amorphous silicon, dopant activation, and laser versus electron beam heating follows. A postulated mechanism for pulsed solid phase annealing is also given.

2.3.2 Energy Deposition

An electron incident upon a solid loses energy through ionizing and radiative collisions, and is scattered by elastic collisions. At energies below 100 keV an electron has insufficient energy to damage the crystalline silicon lattice by causing an atomic displacement. Also, because silicon is a low atomic number material, radioactive collisions are rare and the conversion of electron energy to x-rays is between 10^{-4} and 10^{-3} and can be neglected. Thus the path of an electron in silicon can be modeled by a random walk based upon known scattering probability with an average, uniform energy loss per unit path length.

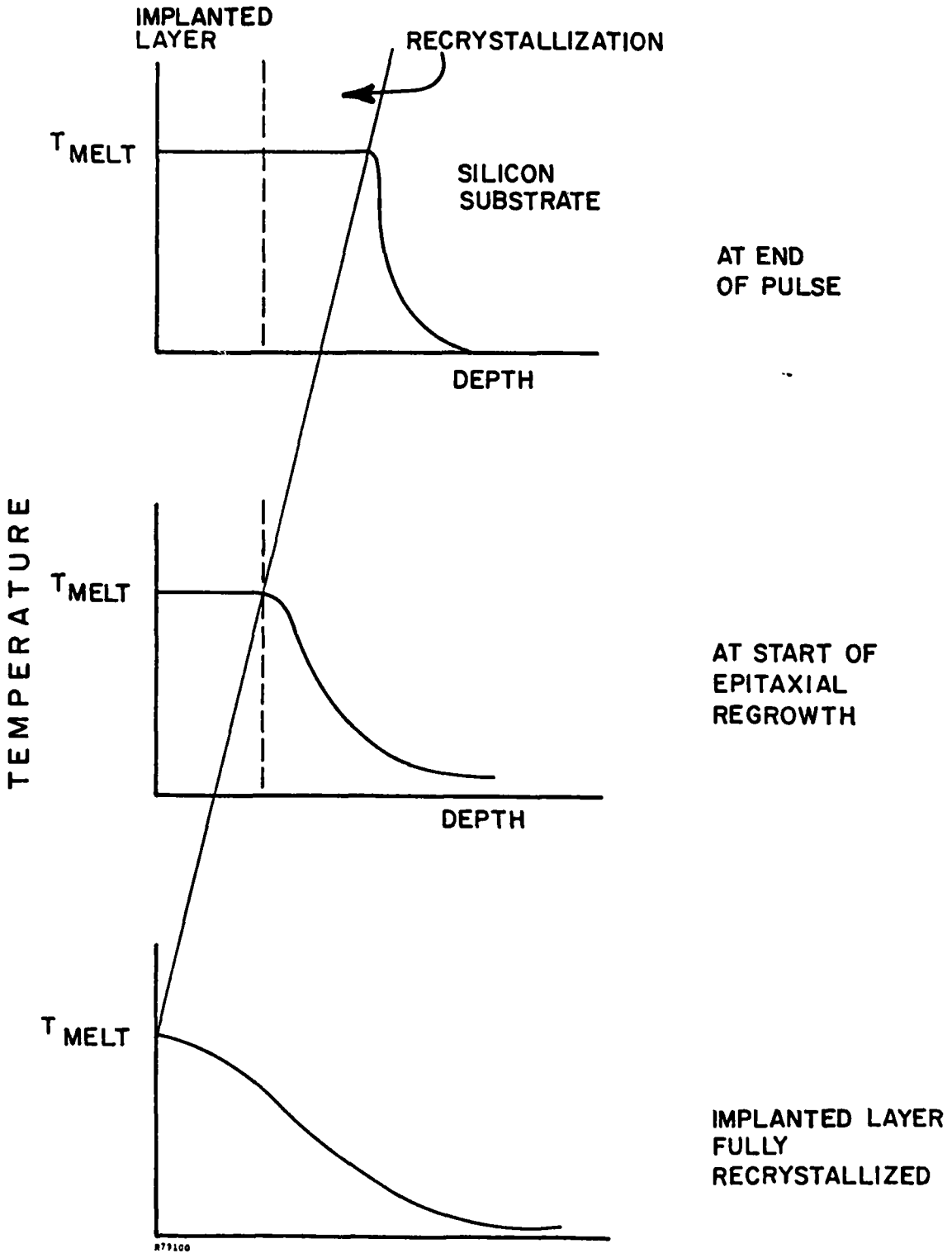


Figure 1. Thermophysical model of pulsed electron beam annealing of ion implantation damage by liquid phase epitaxy.

Using this model, the depth-dose profile of energy deposited in silicon was calculated for the appropriate energy spectrum and angle of incidence (Figure 2). The Monte Carlo calculation was performed by the computer code ELTRAN.[11] The accuracy of this code for the materials and energy range of interest has been checked.[12] Units for absorbed energy have been normalized to a fluence of 1 J/cm^2. Backscattered electrons have been subtracted from the data presented. Note that this depth dose profile is temperature independent.

The data in Figure 2 can be interpreted on a simplistic thermal model. The temperature of the silicon sample after irradiation can be found by multiplying the absorbed dose (given in Figure 2) by the fluence in J/cm^2 and dividing by the specific heat of silicon in $J/g^{\circ}C$. Thermal diffusion and phase changes are neglected.

The effect of a thin-oxide film on electron beam deposition is also shown in Figure 2. It is assumed that the oxide would be used as a mask for ion implantation and pulse annealing. It is designed to prevent the electron beam from melting covered silicon material when exposed silicon surfaces would be melted by the beam. As shown in Figure 2, the 0.5 micron oxide film has reduced the peak energy deposited in the silicon by half. Because the thermal conductivity of the oxide is low, the absorbed thermal energy will be partially radiated away and transferred to the substrate too slowly to initate melt. Most incident electrons (the integral under the curve) will pass through the oxide and stop in the silicon substrate. Very little charge will remain trapped in the oxide because radiation induced conductivity is sufficient to turn the insulating layer to 100 ohm-cm material during the electron beam pulse.

2.3.3 Thermophysical Model

A thermophysical model was developed to explain the observed motion and activation of the dopant. Duration and velocity of the liquid-solid interface (Figure 1) were the parameters sought.

Temperature profiles were calculated by the code VXTEMP[9], developed at Spire Corporation, which solves the thermal diffusion equation using a finite element approximation. This approach allows the use of temperature dependent parameters such as thermal conductivity, heat capacity, and radiated energy. The code uses a time-dependent electron flux with the constant deposition profile shown in Figure 2.

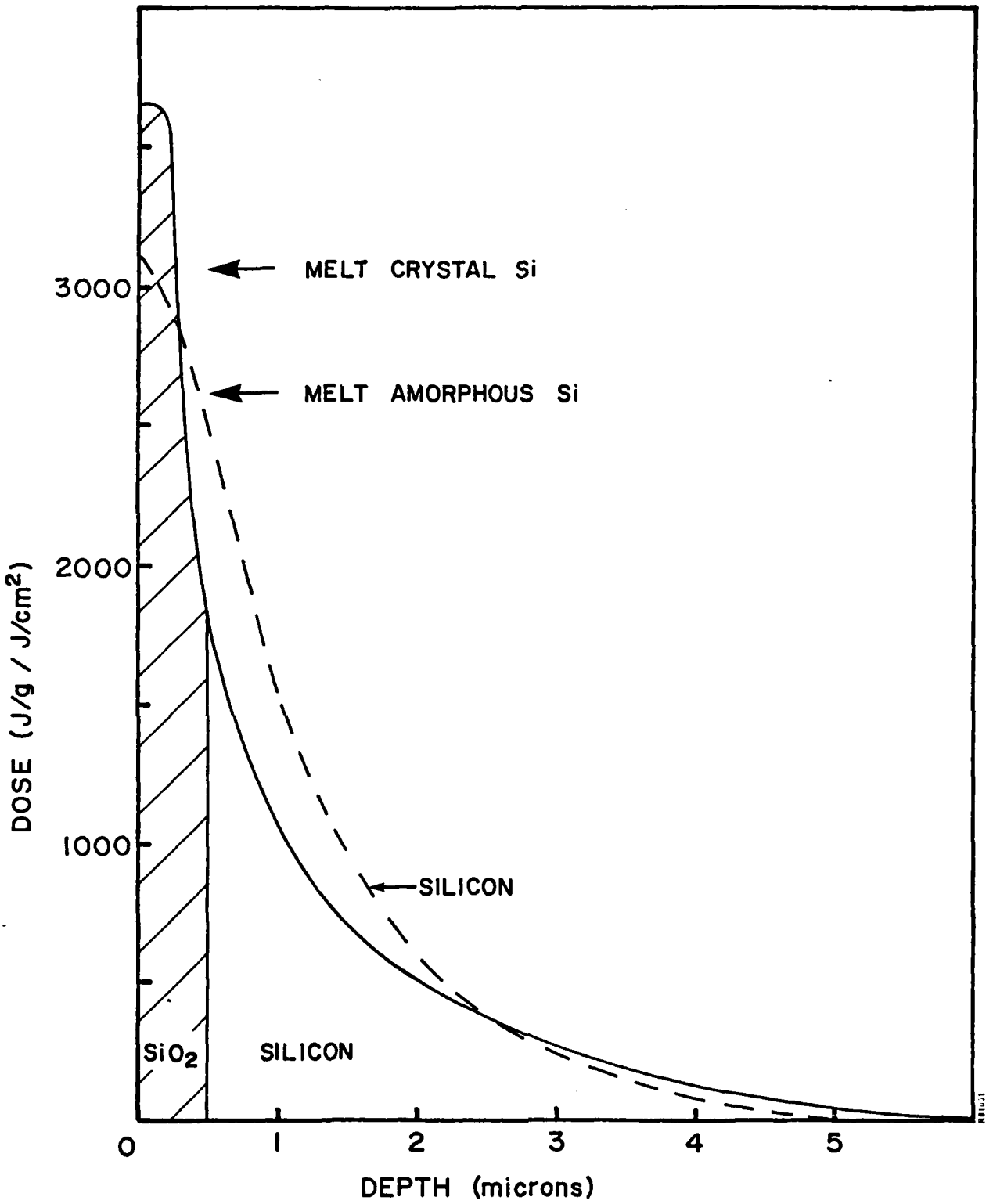


Figure 2. Electron energy deposition profile in silicon, and in silicon covered by 0.5 micron of oxide, showing how the reduction in absorbed dose prevents melting under the film. Normalized to 1 J/cm^2 fluence.

Use of this energy deposition profile implies that the energy transfer from the primary incident electrons to the lattice is instantaneous. Diffusion of energy through carriers other than phonons is negligible. (Note that this is not necessarily true when lasers are used to heat silicon.) Also, the energy in backscattered electrons is considered lost, even though the strong electric fields of the intense electron beam can reflect such particles back into the material. This 10 percent effect cannot be accurately computed.

The thermal properties of the implantation damaged surface must be considered. If the surface is heavily damaged and amorphous, then the free energy in the change from the random to the ordered state (1082 J/g) must be recovered upon heating.[13] In VXTEMP, this energy is added to the appropriate layer when it reaches the melt temperature (1410^{o}C) reducing the effective heat of fusion. In addition, some authors[14,15] have proposed that the amorphous layer melts at a lower temperature. It is clear that an amorphous surface layer requires a lower fluence in the pulsed beam to initiate melt, but the exact thermal model remains uncertain at this time.

Results of this calculation are shown in Figure 3. The substrate was assumed to be single crystal silicon with a one micron amorphous silicon surface. The entire surface layer was to be melted by a pulsed electron beam with an 80 ns pulse width (Gaussian profile) and a total fluence of 1.6 J/cm^2. Calculated temperature histories at different depths are shown as a family of curves in Figure 3, with the temperature plotted against log time. The change in phase at the vaporization point was ignored.

The calculation shows that a broad band of material melts very rapidly and cools more slowly. When the surface reaches the melt temperature, it remains at that temperature until it receives additional energy to make up the heat of fusion (non-equilibrium thermodynamics). This is possible with electron beam irradiation because energy is deposited in a broad region. Once the heat of fusion is absorbed, a 0.5 micron thick band of material melts in 5 ns (Figure 3). This establishes a liquid-solid interface which propagates inward by thermal diffusion with additional heating. The velocity of this interface now exceeds 10 m/s. When the heat source is removed, cooling occurs primarily by thermal conduction to the thick substrate. During cooling the velocity of the liquid-solid interface back towards the surface is lower, about 1 m/s. Solidification of the surface occurs in 2 microseconds.

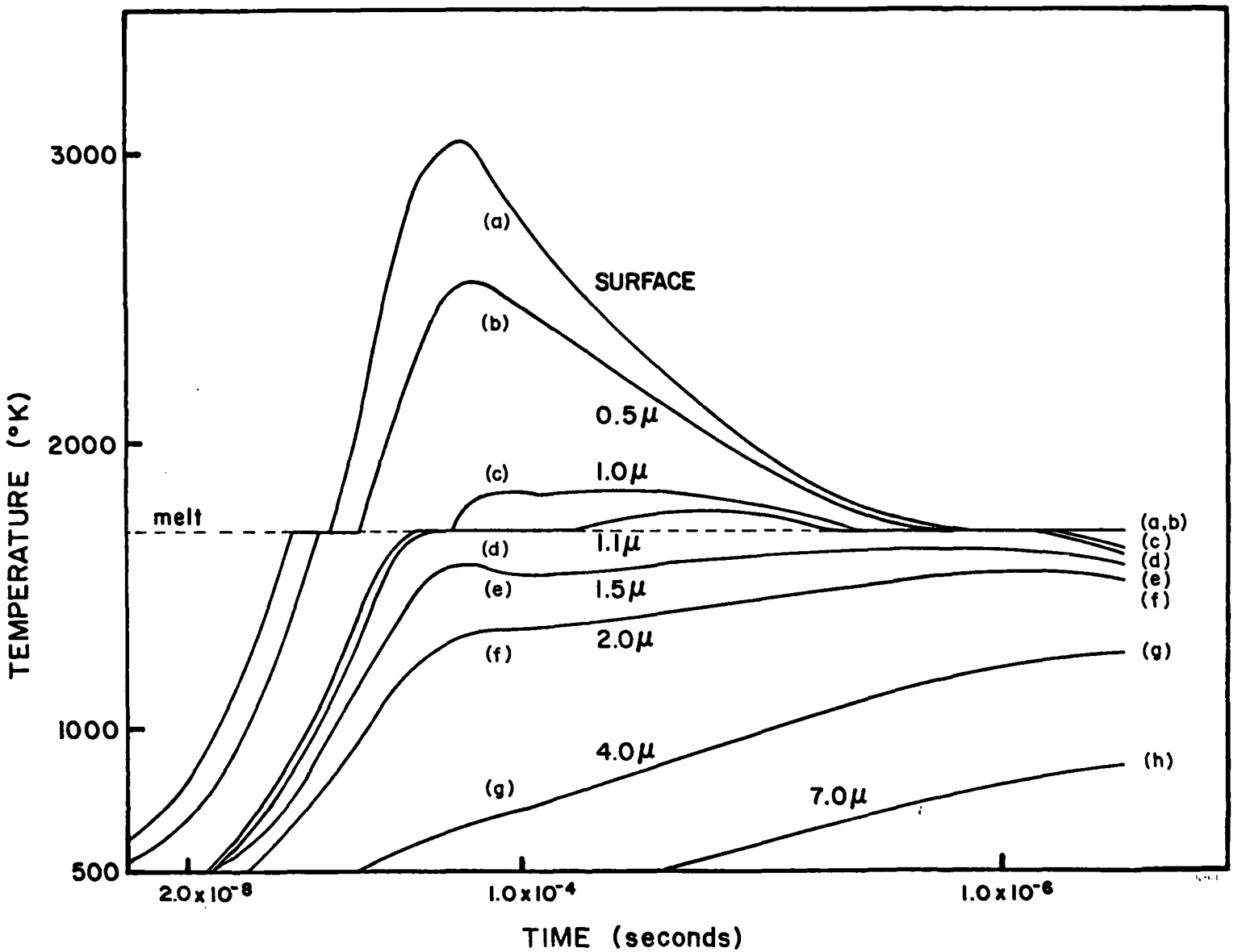


Figure 3. Calculated temperature time profiles for different depths (given in microns) for PEBA of silicon. Surface was 1.0 micron amorphous silicon on a crystal silicon substrate, heated by an 80 ns pulse at 1.6 J/cm^2.

A significant difference between electron and laser beam pulsed heating can be inferred from Figure 3. With lasers, as soon as the surface reaches the melt temperature all light energy not reflected is absorbed in a layer about 10 nm thick (for wavelengths shorter than 1 micron). This 10 nm layer melts, and a melt front diffuses into the material. For electron beam heating, the minimum melt depth would be about 0.5 microns for the beam parameters indicated.

Lateral diffusion of the melt front was not modeled in this program. However, the velocity of the solid-liquid interface would be lower in a region that was shielded from irradiation (by an oxide film) compared to vertical motion into a region that had been heated by direct deposition of electron energy. Therefore, lateral diffusion of dopant under an oxide film edge would be less than vertical diffusion of the dopant during liquid phase PEBA.

Once the heat source is removed and the surface begins to cool, thermal calculations show no difference between laser and pulsed electron beam heating except that the latter has deposited much more energy deeper into the material. This reduces the velocity of the solid-liquid interface, comparing electron to laser beam heating, as it moves toward the surface. Modeling of phenomena at this interface during cooling has been examined by many authors.[16,17] Conduction of heat to the substrate is so rapid for crystalline silicon that the liquid near the interface will be undercooled (i.e. below melt temperature). This increases the growth rate of the crystal. Since crystal growth at the solid interface is much faster than random nucleation, epitaxial regrowth is assured.

2.3.4 Model of Dopant Motion

Incorporation of dopants into the crystal at the rapidly moving liquid-solid interface during cooling is very different than in near equilibrium conditions. Rejection of dopants from the solid back into the liquid is limited by the diffusion rate in the liquid away from the interface. Dopants can therefore be incorporated into substitutional positions in the lattice in excess of the solid solubility. At extreme dopant concentrations, in excess of 10^{21} atoms/cm^3, instabilities in crystal growth due to constitutional supercooling can lead to non-epitaxial cellular crystal growth.[17] However, this range of dopant concentration is not now encountered in integrated circuit processes for single crystal silicon.

Redistribution of dopants during pulse annealing occurs only in the liquid phase. Diffusion coefficients for dopants in liquid silicon at 1410°C are approximately 3×10^{-4} cm^2s, or six- to ten-orders of magnitude larger than diffusion coefficients for common dopants (As, B, Ga, In, P, Sb) in the solid phase.[18] For the duration of high temperatures in PEBA, less than 10 microseconds, solid state diffusion can be neglected.

Implanted dopants are initially in a very thin layer near the wafer surface. After PEBA irradiation, the surface is melted past this depth to insure good crystal regrowth (damage may extend below implanted dopant). The dopant diffuses into the molten silicon, flattening the peak concentration without creating a long tail. During crystal regrowth the dopant is frozen into substitutional positions in the crystal lattice. The rapid motion of the liquid-solid interface does not zone refine arsenic, boron, or phosphorus at concentrations below 10^{21} atoms/cm^3. Other dopants (such as In, Ga, or Sb) may be zone refined to the surface[17], but this was not observed in this experiment.

2.3.5 Solid Phase Epitaxy

For those cases where no diffusion of the dopant can be tolerated, a pulsed solid phase anneal mechanism was proposed. This solid phase epitaxy (SPE) model is based upon the two cycle furnace anneal mechanism.[19] A low temperature (500-600°C), long time (60-120 minutes) heating cycle is used to restore the crystalline structure of the implanted material. A high temperature cycle (850-1000°C) for a short time (10-15 minutes) follows to activate the dopant and to reduce the concentration of point defects. In a furnace anneal the advantage of two cycles is realized when a high dose implant has created heavy (amorphous) surface damage. In this region random nucleation can occur at high temperature which will damage the final crystal structures. Random nucleation does not occur in an anneal at low temperature, so that the crystal structure is better with two cycles than in an all high temperature anneal.

To anneal ion implantation damage without melting by SPE, a certain temperature-dependent time is required to regrow the crystal structure. The minimum time, for temperatures near melt and typical implants, is 10 microseconds.[20] Without melting, the short 100 ns pulse from Spire's equipment can not maintain a high surface temperature for the required duration. The alternate technique uses the low temperature furnace anneal to regrow the crystal lattice, and a short, non-melting pulse to replace the high temperature furnace anneal. Annealing point defects and activating dopant, by forcing atoms from interstitial positions to substitutional ones, should require

less time than rearranging the atoms in a finite thickness layer. This model is just a proposed explanation.

2.4 PEBA FOR DIFFERENT IMPLANT PARAMETERS

2.4.1 Objective

The objective of this work was to determine how to pulse anneal ion implants in single crystal silicon typical of integrated circuit technology. Prior experience with PEBA was confined mostly to annealing low energy, high dose ion implants related to solar processing.

The approach was to work through a matrix of different implant parameters using different annealing cycles to optimize results. Best results were obtained when pulsed heating was combined with low temperature thermal cycles.

2.4.2 Optimum Anneal Cycle

The test matrix consisted of ion implants at energies between 25-200 keV with doses between 10^{13} to 10^{16} ions/cm^2. Combinations of ion (As, B, P and BF_2), energy and dose used are given in Table 1. Additional data for low energy, high dose implants of boron, phosphorus, and BF_2 were made available from device processing tests.

The optimum pulse anneal cycle for all implants was a high fluence (melting) pulse anneal of a heated (400°C) sample. Equally good results were obtained for samples pulsed at room temperature, followed by a 550°C thermal anneal. The effect of an anneal at 550°C before pulsing was uncertain.

The matrix of different annealing procedures tested is shown below:

1. Pre-pulse: None, or 550°C for 2 hours
2. PEBA: Sample temperature 20°C, 400°C
   Fluence 0.6 to 1.6 J/cm^2
3. Post-pulse: None, or 550°C for 2 hours

Not all types of anneal treatments were performed for all implants. The low temperature furnace cycle (550°C for 2 hours) was choosen because it is sufficient to restore the crystal structure of a heavily damaging implant[19]. The fluence of the pulsed beam ranged from non-melting to the damage threshold.

Table 1

Implantation matrix for PEBA experiments.

Ion Dose (cm^{-2})	Ion Energy (kev)			
	25	50	100	200
10^{13}	As, B	—	B	—
10^{14}	As, B, P	—	As, B, P	—
10^{15}	As, B, P, BF_2	B, P, BF_2	As, B, P	As, B,P
10^{16}	As, B, P, BF_2	BF_2	As, B	—
Substrates:	(100) and (111) from 0.1 to 20 ohm-cm n-type for B, BF_2 p-type for As, P			

The fluence required for optimum pulse annealing varied with all implant parameters. There are two effects discussed more fully in the following sections. First, the threshold fluence required to initiate melt was lower for amorphous silicon surfaces when compared to crystalline silicon results. Second, because the melt depth must extend below the implantation profile to fully activate the dopant, the fluence must be increased for higher energy implants or implants of boron (compared to phosphorus or arsenic).

A damage mechanism at high fluence limits the maximum depth of silicon which can be melted, and the implants which can be annealed, with one set of electron beam parameters. For this experiment, very low electron energies and a high angle of incidence were chosen beam parameters to melt the minimum thickness layer. As the fluence was increased the surface was overheated relative to deeper layers, pitting by possible vaporization occurred above 1.6 J/cm^2. Also, the thermal gradient was very high and stress created slip in (100) wafers above 1.4 J/cm^2. The threshold for slip in (111) wafers was lower.[21] A change in electron beam parameters can be made for melting deeper layers without damage, as discussed in Section 3.2.3.

2.4.3 Annealing Amorphous and Non-Amorphous Surface Damage

A comparison of results of PEBA for implants which leave the surface amorphous or non-amorphous is shown in Table 2. Boron fluoride (BF_2) implants were heavily damaging, while the boron implants were not as damaging. This was easily confirmed by the optical properties (color) of the as-implanted surfaces. These implants were chosen because the active ion (boron) would be the same in both cases. The energy of the boron and BF_2 ions was chosen such that the implant profile of boron would be nearly the same.

Annealing of these implants is shown in Table 2 as a function of the thermal cycling of the sample:

1. Low temperature thermal anneal only, 550°C for 2 hours.
2. High temperature thermal anneal at 950°C for 30 minutes, following (1).
3. PEBA treatment following (1).
4. PEBA alone.
5. PEBA followed by cycle (1).

The fluence for pulsed annealing by PEBA, 1 J/cm^2, was just above the melt threshold for crystalline silicon.

Table 2

Results of PEBA on amorphous (BF_2) and non-amorphous (boron) ion-implant damaged surfaces. Sheet resistance R (ohms/square) measured by 4-point probe, photovoltage V_{oc} (mV) measured by point probe in AM0 illumination.

Anneal Cycle Temp./Time (°C/minutes)	5 keV ^{11}B 5E15/cm^2		25 keV, $^{49}BF_2$ 5E15/cm^2	
	R (Ω/□)	V_{oc} (mv)	R (Ω/□)	V_{oc} (mV)
550/120	136	440	131	331
550/120 950/30	55	530	59	517
550/120 1 J/cm^2	29	495	47	470
1 J/cm^2	26	400	25	530
1 J/cm^2 550/120	36	520	65	525

Measurements were made of sheet resistance and point probe photovoltage (V_{oc}) with an open circuit. Readings of V_{oc} are for comparison only, with low values being an indication of defects. It was found that good solar cells could only be fashioned if the V_{oc} value exceeded 500 mV, with the voltage of the final completed cell being higher. Readings of sheet resistance are an indication of the percent of activation of the dopant. The calculated value for sheet resistance assuming full activation and no dopant diffusion was 24 ohms/square. About half of the implanted dopant was at a concenentration above the solid solubility of boron in silicon.

The low temperature thermal anneal was insufficient to activate the dopant of these implants. After this treatment, the sheet resistance was very high and many point defects remained.[22] The sheet resistance was lowered by heating at 950°C, but this did not fully activate the dopant for concentrations in excess of the solid solubility limit. The fact that the sheet resistance was equal to the calculated value for very high dopant concentrations after PEBA, and increased after further thermal heating at 550°C, implied that PEBA did activate dopant in excess of the solid solubility limit (with the excess boron precipitating after low temperature heating) and did not diffuse the dopant to lower concentrations prior to activation.

The interpretation of the V_{oc} data is based upon the assumption that PEBA at 1 J/cm^2 did not melt crystalline silicon deep enough to remove damage in the tail of the implant (e.g. boron implants or BF_2 with low temperature pre-pulse anneal). PEBA did melt the surface. This improved the crystal structure in the damaged region and activated most of the dopant, which lowered the sheet resistance. But point defects under this layer caused a low V_{oc} reading. By comparison, PEBA at the same fluence melted a deeper layer when the surface was amorphous (BF_2 implant without pre-anneal) and this reduced the defect density further, improving V_{oc}. Many of these defects were annealed by a low temperature thermal cycle after PEBA, and their effects reduced by such a thermal cycle before PEBA.

This is not the only plausible explanation of the data. The damage implied by V_{oc} measurements could have been caused by pulsed heating of a crystalline surface. Characterization of these defects was performed when fabricating devices, Section 2.6.

2.4.4 Annealing Different Implant Doses

PEBA results did not vary with ion implantation dose if the surface of the sample remained crystalline in character. This restriction implies that for irradiation at a constant fluence, the melt threshold and melt depth would not depend upon implanted dose. Types of defects encountered do vary with implant dose, but this would not affect a liquid phase anneal. By comparison, pulsed laser annealing did vary with implant dose under the same conditions.[23]

Boron was implanted at 25 keV into (111) silicon at 10^{14} and 10^{15} ions/cm^2. At higher doses the solid solubility limit was exceeded, see Section 2.3.3. At lower doses there was some difficulty in making contact to the implanted area, therefore an implant at 10^{13} ions/cm^2 was tested when making resistors because a separate contact implant was provided. Samples were annealed by a variety of thermal cycles as in Section 2.3.3, but emphasis was placed on varying the beam fluence (see Table 3).

Table 3

Sheet resistivities for 25 keV boron implants into (111) silicon comparing the effect of varying fluence and low temperature preannealing on PEBA.

Anneal Cycle Temp./Time or fluence (°C/min.) or (J/cm^2)		R_s (ohms/sq.) for 10^{14}/cm^2	R_s (ohms/sq.) for 10^{15}/cm^2
550/60	—	2230	1269
550/60	0.8	1460	—
550/60	1.1	810	160
550/60	1.4	720	—
—	1.1	725	167
—	1.4	720	131
550/60, 950/15	—	717	125
calculated		688	93

Boron concentration profiles were measured by secondary ion mass spectroscopy[24] or SIMS analysis. Relative concentration was initially plotted as a function of sputtering time in Figure 4. Depth scales were fitted from measurements of (flat) sputter crater depth, and are accurate assuming a constant sputter rate. Boron profiles as-implanted and after a low temperature anneal (550°C for 1 hour) are nearly identical and indicate no diffusion; the slight differences between these curves could be attributed to errors in transposing data onto different scales. After a high temperature anneal at 950°C for 1 hour, the junction has diffused inward about 0.1 micron and the peak of the profile flattened. This can be understood from concentration enhanced diffusion rates.[25]

The boron profile after PEBA implies that the melt depth was either very close to, or not as deep as the tail of the implanted distribution. Pulse annealing occurred after the 550°C anneal, and the data in the tail of this profile should be interpreted as being coincident with the as-implanted and low temperature anneal curves. The flattening of the peak concentration implies melting. Lack of diffusion in the tail region shows that the melt depth was less than or equal to 0.3 microns (approximately).

The data in Table 3 give the sheet resistance for these implant and anneal cycles. As the fluence of the electron beam was increased the sheet resistance dropped, finally reaching the value in a high temperature thermal anneal (950°C for 15 minutes) at 1.4 J/cm^2. The sheet resistance was very high for the low temperature thermal anneal and the low fluence pulse anneal. The calculated values of the sheet resistance assume full activation and a Gaussian dopant profile. Differences between this value and the high temperature thermal anneal sheet resistance are minimal.

Using these data, and the boron profiles in Figure 4, it was surmised that 0.8 J/cm^2 was close to the threshold value for melting crystal silicon for these beam parameters. For this fluence, the low total amount of boron activated may have been due to a fast solid phase anneal mechanism. At higher fluences, the silicon surface did melt but not as deep as the junction (at about 0.6 microns). Some amount of boron was not activated, even at 1.4 J/cm^2 which was near the damage threshold. The sheet resistance drops with increasing fluence because the increasing melt depth activates more of the dopant in the tail region of the implant. There does not appear to be a difference in PEBA results, comparing the percent of boron activated against the high temperature thermal anneal, between the implant doses of 10^{14} or 10^{15} ions/cm^2.

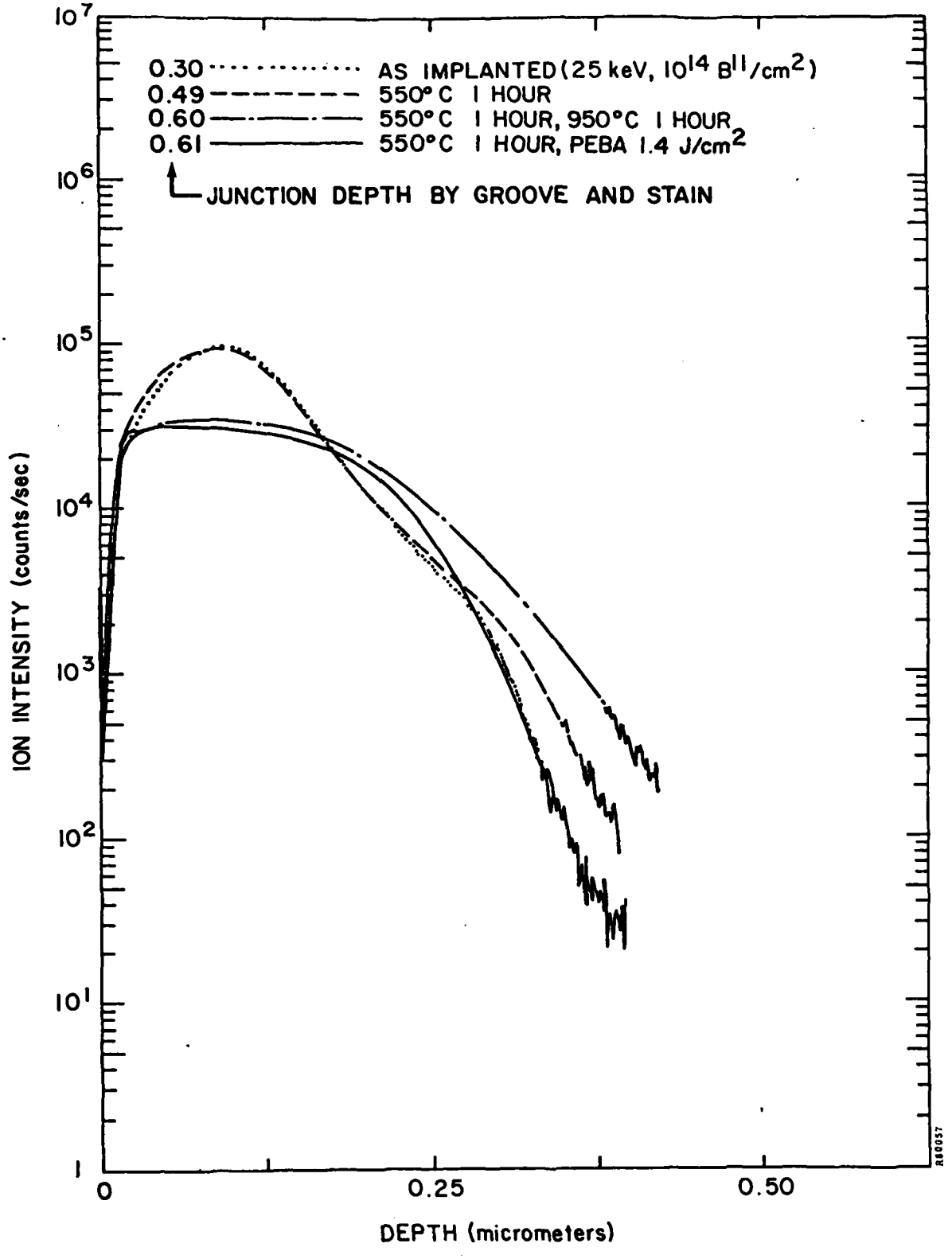


Figure 4. SIMS profiles of boron implanted into silicon showing relative motion of the dopant for various anneal cycles. Junction depth measured by groove and staining.

This experiment shows results similar to pulsed laser annealing, Table 4. These data were published after Spire completed the experiments, so that a direct comparison at identical implant energies was not possible.[23] For the wavelength of laser used, and pulse width (20 ns), the threshold for melting occurred near 1.5 J/cm^2. Above this level the sheet resistance drops with increasing fluence for 10^{14} ions/cm^2 dose. At 10^{15} ions/cm^2 the sheet resistance stabilized over 2.0 J/cm^2. Lower sheet resistance values were obtained for thermal annealing at high temperatures than for pulsed laser anneals.

One difference between pulsed laser and pulsed electron beam annealing can be seen comparing Tables 3 and 4. The absorption of laser light increases with ion implant dose, so that the melt depth for 10^{15} ions/cm^2 was probably below the boron as-implanted profile at 2.0 J/cm^2 and the sheet resistance measurement did not change after that. For the lower dose implant (10^{14} ions/cm^2) the melt depth did apparently increase with fluence between 2.0 and 2.5 J/cm^2. The change in melt depth did not occur with electron beam heating for a change in implant dose when the surface remained crystalline. Laser annealing was more sensitive to this parameter.

Table 4

Sheet resistance (ohms/square) of 50 keV boron implanted silicon annealed by a pulsed ruby laser.[23]

Anneal Fluence (J/cm^2)	10^{14} ions/cm^2		10^{15} ions/cm^2	
	(111)	(100)	(111)	(100)
1.0	*	*	3372	5312
1.5	975	1712	406	280
2.0	907	877	124	127
2.5	794	866	124	128
1000°C, 10 min	655	619	109	113

*Readings too high to be reliable

2.4.5 Annealing Ion Implant Damage for Different Energies

Variations in PEBA results, for annealing ion implant damage with varying ion energy, were consistant with the model that the melt depth should exceed the maximum penetration of the implanted ions. Implants were performed at constant, low doses so that the silicon wafer surface remained crystalline. There was no change in the threshold fluence of the electron beam to initiate melt, and there was no change in the melt depth at constant fluence. However, activation of the dopant after pulse annealing could be correlated with the amount implanted above or below the expected melt depth.

Two experiments were performed. In one case, boron was implanted to a dose of 10^{15} ions/cm^2 at 25, 50, 100 and 200 keV. These implants were through large openings

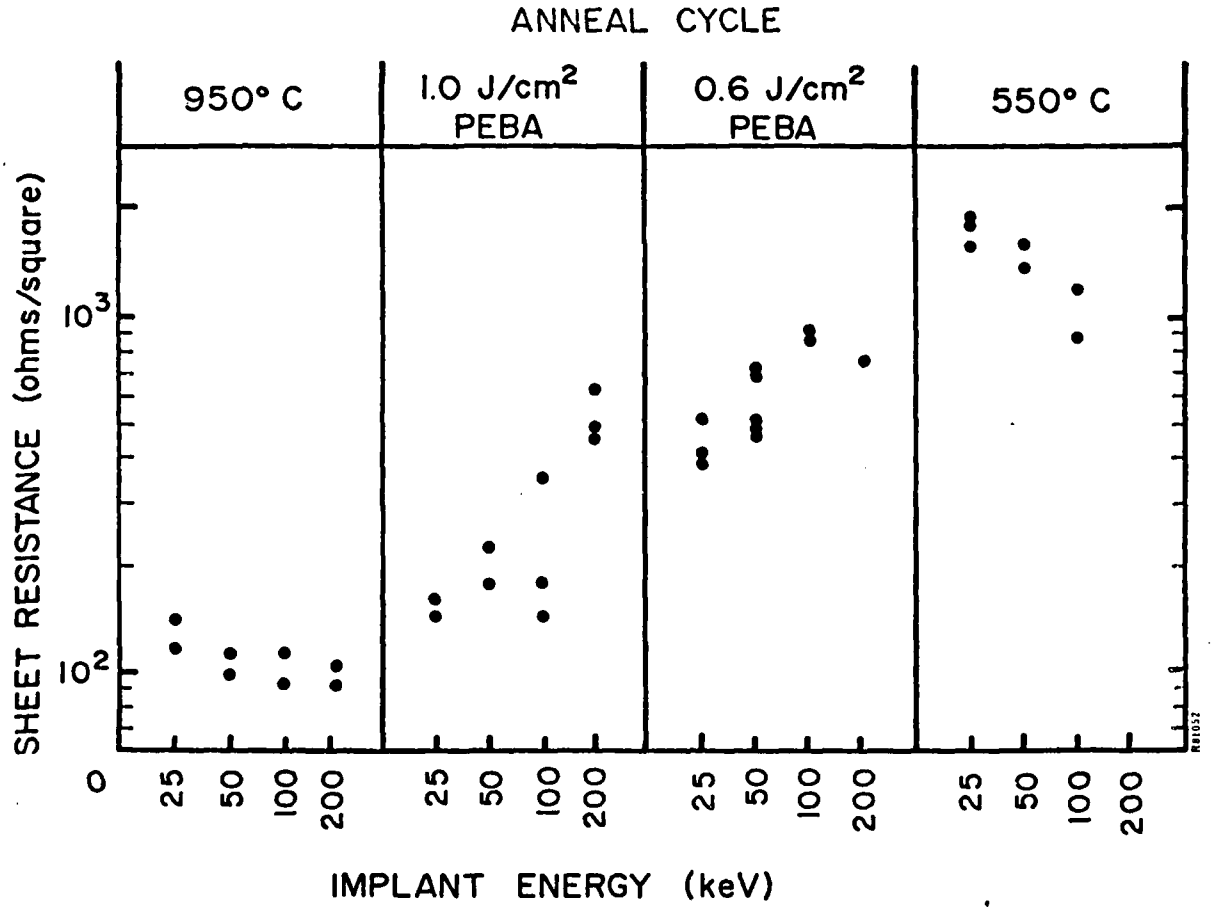


Figure 5. Sheet resistance for boron implants at 10^{15} ions/cm^2 and varying ion energy. Anneal cycle was 550°C for one hour, followed by the given cycle, followed by 550°C for one hour.

(1.59 x 6.35 mm) in a thick oxide film. Opening size was adjusted to give correct sheet resistance values for a given four-point probe spacing. Most of the area on the waferwas used for device tests (Section 2.6). Measured sheet resistance results are given in Figure 5 for various anneal cycles.

In the second test, phosphorus was implanted to a dose of 10^{14} ions/cm^2, at 25 and 100 keV, into the whole wafer surface. The lower ion dose was required to prevent amorphous damage to the wafer surface. Measured sheet resistance results are given in Table 5 as a function of anneal cycle. Note that the minimum required temperature for full activation of phosphorus in a two cycle anneal (850°C) is lower than that required for boron (950°C). Calculated sheet resistance values were very close to the measured values for high temperature thermal anneals.

Annealing by PEBA at a fluence of 1.0 J/cm^2 was sufficient to activate most of the dopant for either implant in Table 5. For the 25 keV phosphorus implant, the dopant could have been redistributed to a greater average depth, resulting in higher mobility and lower sheet resistance. In Figure 5, however, only the shallow 25 keV boron implant showed significant dopant activation at this high fluence.

Annealing by PEBA at a lower fluence of 0.6 J/cm^2 activated 0 - 20 percent of the boron and possibly as much as 60 percent of the phosphorus in these experiments. For the deep implants (100 and 200 keV boron) there was no measurable increase in activation after PEBA compared to results of the low temperature thermal cycle.

Table 5

Sheet resistance measurements for phosphorus implants at 10^{14} ions/cm^2 and varying energy and anneal cycles

Anneal Cycle (550°C for 2 hours) followed by:	Sheet Resistance (ohms/square) 25 keV	100 keV
pulse at 0.6 J/cm^2	689	567
pulse at 1.0 J/cm^2	354	318
850°C/15 min	505	298

These sheet resistance measurements were correlated to the estimated melt depth of PEBA and the implant profile. The implanted dopant profile is reasonably approximated by the LSS theory, except for uncertain channeling effects which give a deep tail at low concentrations. These calculated profiles have tabulated Gaussian approximations[26] given in Table 6. Assuming that all the dopant in the melted surface region would be activated by PEBA, the percent of dopant activated is given approximately by the integral under the Gaussian curve to the estimated melt depth. These figures are shown in Table 6. The estimated melt depth at 1.0 J/cm^2 is between 0.25 and 0.3 micron. For 0.6 J/cm^2 the estimated melt depth is less than or equal to 0.12 micron.

Measured activation given in Table 6 is the ratio of the sheet resistance from a high temperature thermal anneal, to the measured sheet resistance for the pulse fluence given in Figure 5 or Table 5. This measured value is roughly in agreement with the calculated values based upon estimated melt depths.

The choice of the low fluence, 0.6 J/cm^2, was based upon calculations implying that it was below the melt threshold for crystal silicon. At slightly different beam parameters,[15] this fluence did not melt crystalline silicon. Without the measured dopant profile, there is no sure way to identify melting or non-melting in this experiment. In fact, the increase in activation of the dopant at 0.6 J/cm^2 may be due to the solid phase anneal mechanism proposed in Section 2.3.5.

Table 6

Activation for various melt depths, calculated as integral of Gaussian fit to implanted dopant profile from LSS theory, or measured from sheet resistance of PEBA experiments

Ion	Energy (keV)	Projected Range (micron)	Standard Deviation (micron)	Percent of Dopant Less Than: 0.12μm	0.3μm	Percent Measured Activation 0.6J/cm^2	1.0J/cm^2
P	25	.0311	.0143	99	99	73	100
P	100	.1238	.0456	47	99	53	100
B	25	.0825	.0327	87	99	25	100
B	50	.1608	.0504	21	99	17	60
B	100	.2994	.0710	0.6	50	0	50
B	200	.5297	.0921	—	0.6	0	0

2.4.6 Annealing Heated Samples

Changes in PEBA results with low temperature (550°C) pre-pulse or post-pulse heating led to the investigation of pulse processing a hot sample. A thermally-isolated but electrically-grounded sample holder was constructed which could be radiantly heated to 400°C. The sample could be moved into position and pulsed within 30 seconds after reaching the desired process temperature. The measured temperature drop during this delay was less than 30°C. Initial experiments determined the effect of temperature cycling at 400°C compared to pulse processing a wafer heated to this temperature. A second test combined pulse annealing heated samples with the 550°C cycles previously used.

One concern was whether or not heating a sample to 400°C before or after pulse annealing would have the same effect as pulse irradiating a sample at 400°C. Samples were prepared by implanting phosphorus at 10 keV to a dose of 2.5×10^{15} ions/cm^2, creating amorphous surface damage. These wafers were annealed by the various cycles shown in Table 7, after which the sheet resistance and point probe open circuit photovoltage were measured as described in Section 2.4.3.

The sheet resistance for any PEBA cycle in Table 7 is much lower than that measured for the short-time, high-temperature furnace anneal. Heating at 400°C after PEBA did not increase the sheet resistance. Heating at only 400°C activated a minimal amount of dopant. The peak concentration of phosphorus as-implanted was above 1.4×10^{21} atoms/cm^3. With minimal diffusion, the furnace anneal did not activate dopant at concentrations in excess of the solid solubility limit at 850°C, approximately 4×10^{20} atoms/cm^3. During PEBA the dopant was redistributed in the melt phase to lower concentrations and fully activated. Since the sheet resistance did not change with further heating, compared to boron results in Section 2.4.3, the concentration of phosphorus is presumed to be less than or equal to the solubility limit.

The drop in photovoltage from the maximum value (560 mV) in Table 7 was interpreted as showing defects in or near the junction region (Section 2.4.3). The difference between the thermal cycles for PEBA in Table 7 is shown by V_{oc} values. PEBA alone activated the dopant but left some defects reducing V_{oc}. Radiant heating to 400°C after PEBA in vacuum increased V_{oc} to near the maximum value. Pulsing a wafer heated to 400°C, however, kept V_{oc} at the maximum value. Pulsing a wafer at lower temperature (250°C) had no significant advantage over PEBA at room temperatures.

Table 7

Effects of heating sample during PEBA of a high dose implant with amorphous surface damage.

Thermal Cycle	Sheet Resistance (ohms/sq.)	V_{oc} (mV)
Heat to 400°C in 10 min, cool	276	505
Heat to 400°C in 10 min, Cool to 250°C in 5 min, pulse	21	525
Heat to 400°C in 10 min, Pulse at 400°C, cool	18	558
(repeat)	19	555
Pulse (only)	19	518
Pulse, then Heat to 400°C in 10 min, cool	20	545
(repeat)	26	548
Heat to 400°C in 10 min, Pulse at 400°C (30 s), Maintain 400°C for 10 min, cool	20	550
Furnace anneal in N_2 gas 550°C 2 hrs, 850°C 15 min, then 550°C 2 hrs	45	560

Notes: PEBA fluence 1.0 J/cm^2
Radiant heating and cooling in vacuum at 10^{-5} torr, except for furnace.

These results are interpreted as strong evidence that the defects which lowered the value of V_{oc} were created by rapid quenching of solid silicon, near the wafer surface as it cools from melt. These defects appeared to be annealed by a short thermal cycle at 400°C. This is consistant with reported results for annealing defects created by quenching furnace heated wafers in liquid nitrogen.[27] Heating the wafer during pulsing is effective because it reduces the rate of thermal cooling, and because the temperature used was above the reported[27] annealing temperature (350°C) for this type of defect.

In Section 2.4.3 an alternate explanation for the decrease in V_{oc} was proposed. For boron implants, it appeared possible that the melt depth of this fluence was less than the maximum depth of damage in the tail of the implant, and that the defects lowering the value of V_{oc} were unannealed implant damage. In this case, for very shallow phosphorus implants, this was not possible.

A second series of experiments tested the effect of PEBA at 400°C on low dose implants with and without a pre-pulse thermal anneal at 550°C. The results in Table 8 were an extension of the experiment decribed in Table 5. Phosphorus was implanted at 10^{14} ions/cm^2 at either 25 keV or 100 keV. Half of the samples were heated at 550°C for 2 hours, then all were pulse annealed. As outlined in section 2.4.5, the fluence used in this experiment was sufficient to melt through the depth of the 100 keV implant.

Table 8

Effects of heating sample during PEBA of low dose implant.

Anneal Cycle	V_{oc} (mV) 25 keV	100 keV
550°C/2 hrs, PEBA/20°C	349	459
550°C/2 hrs, PEBA/400°C	421	493
PEBA/20°C	339	445
PEBA/400°C	436	460

The value of V_{oc} in this test was affected by dopant concentration. All values were less than shown in Table 8 due to lower concentrations. Meaningful data can be extracted from comparison between PEBA at 20°C or 400°C. The value of V_{oc} is consistantly higher for the heated sample. Pre-annealing the sample at 550°C had a small, possibly beneficial effect. Assuming that the melt depth was nearly identical for the case of 20°C or 400°C PEBA, and that the dopant distribution is about the same, then there is reason to believe that fewer defects were left in the material pulse annealed at higher temperatures.

2.5 PEBA WITH OXIDE LAYERS

2.5.1 Objective

The goal of experiments described in this section was to study the effect of PEBA on patterned structures such as might be found in integrated circuits. Patterned SiO_2 films were used as masks for both implantation and PEBA. The specific questions answered are:

- Does the width of a window (mask opening) affect PEBA?
- Is the oxide (edge, corner, surface, . . .) damaged by PEBA?
- Is there significant lateral diffusion of a junction after PEBA?

The answer to each question is no! The PEBA process is compatible with oxide masks over 0.3 micron thick. Both liquid and solid phase anneal techniques were used with both thermally grown and CVD oxide deposition. Damage to the silicon-oxide interface from the passage of electrons can be annealed.[28]

2.5.2 Ion Implanted Resistors

Ion implanted resistors were used to test PEBA for annealing through varying openings in an oxide mask, and for annealing of very-low-dose ion implants. The geometry of the patterns is shown in Figure 6. The insulating surface oxide (thermally grown) was less than 0.7 micron thick, and the openings etched in it for resistors were 50, 12.5, 5.0, and 2.5 microns wide. Boron was implanted into this oxide mask, at 25 or 100 keV, to one of the following doses: 10^{12}, $3x10^{12}$, 10^{13}, $3x10^{13}$, and $3x10^{14}$ ions/cm^2. This was followed by a second implant at 3×10^{14}/cm^2 into the regions under the contact, as defined by a resist mask. This resist was stripped, and all samples

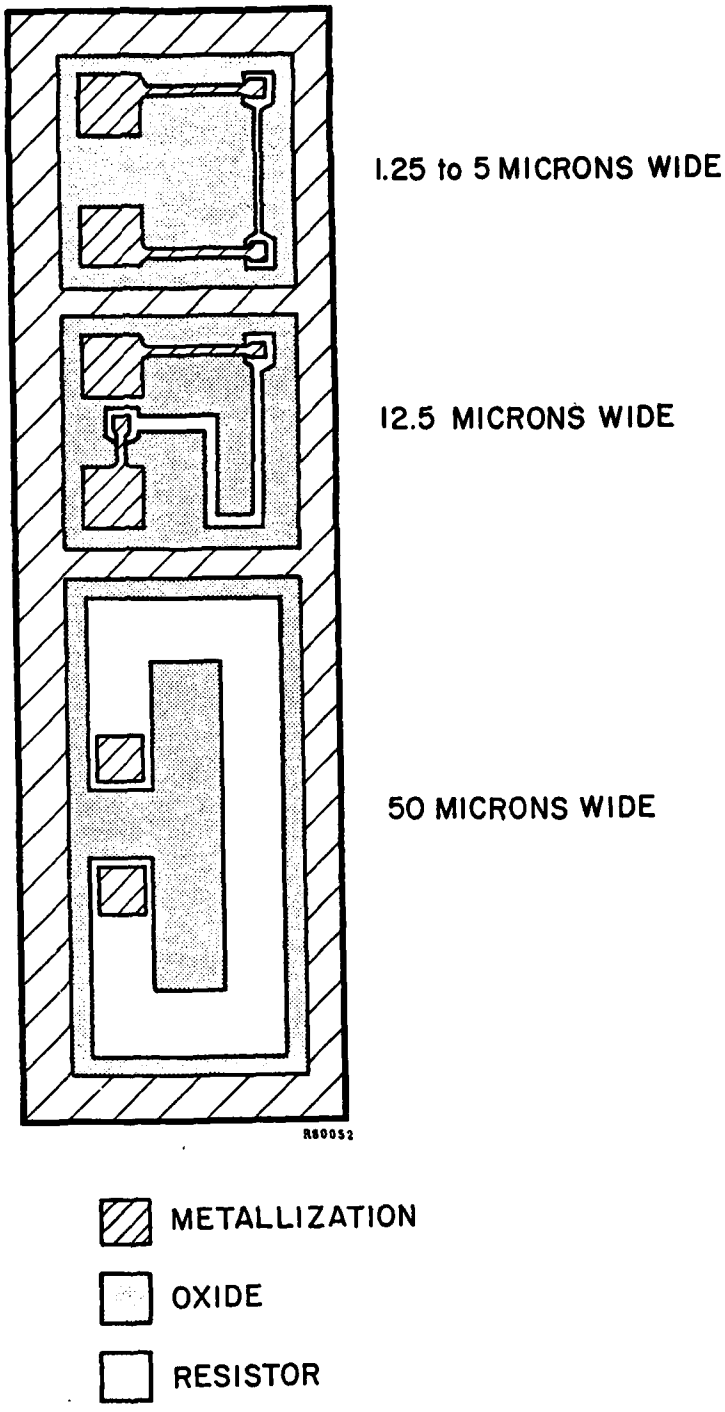


Figure 6. Ion implanted resistor test patterns for analyzing pulsed electron beam annealing with patterned oxides for device structures.

annealed at 550°C for 1 hour prior to pulse processing half of each wafer. High fluence or melting parameters were used, exceeding the damage threshold in some cases. There was no post-pulse anneal other than the sinter of contacts at 480°C for 10 minutes.

The results of annealing as a function of implant dose are similar to the data in Section 2.4.4 for implants above 10^{13} ions/cm^2. Averages over 10 devices were consistent with PEBA reducing the sheet resistance by a factor of two compared to anneal at 550°C only. Compared to 950°C/15 minute anneal, the sheet resistance after PEBA was still high by a factor of two. For lower ion implant doses, 10^{12} or 3×10^{12} ions/cm^2, the sheet resistance after PEBA was anomalously high. These samples did not receive a post-pulse thermal cycle.

The results of annealing as a function of window width are shown in Table 9. The sheet resistance values for all resistors is constant, within 10 percent of the average value. There were no changes observed in uniformity with implant dose above 10^{13} ions/cm^2.

Table 9

Sheet resistance of ion-implanted pulse annealed resistors as a function of oxide window width (25 keV, $^{11}B^+$ at 3×10^{13} ions/cm^2).

Window Width (microns)	Sheet Resistance kilo-ohms/sq
50	3.0
12.5	2.7
5.0	2.75
2.5	2.50

2.5.3 Lateral Diffusion

The experiment on ion implanted resistors contained an indirect test of lateral dopant diffusion. The measured sheet resistance of a resistor with a high length/width ratio would change (become lower) if lateral diffusion affected the width. However, many electrical properties can change the sheet resistance and a comparison between different window widths is misleading.

The test was redefined using a different pattern to determine the possible motion of the dopant directly. A repetitive interlocking finger pattern, Figure 7, was etched into 0.7 micron thick oxide film on a 1-2 ohm-cm boron doped substrate. This sample was implanted with 10^{15} ions/cm^2, 25 keV arsenic. A high dose was chosen to give dopant concentrations in excess of 10^{20} ions/cm^3 for driving the diffusion. After implantation the oxide was removed from half of the sample to check for differences during PEBA where the whole sample surface would be melted, compared to the case where melting was restricted by an oxide mask. Pulse processing was performed at melting and non-melting fluence. In the low fluence case a 550°C, 60-minute thermal cycle preceeded pulsing.

The results are shown in Figure 7. A stain for the n^+ region was used after cleaning the surface and removing any oxide (if present). Figure 7a shows the stain for an implanted, unannealed region. Although most of the implanted arsenic was not substitutional, the stain did attack the implanted region and good resolution was obtained. The effects of annealing under different conditions did not change this pattern appreciably. Figure 7b measured a (one side) junction diffusion of 0.2 micron compared to Figure 7a. The principal error in the measurement was random variation in the width of the etched oxide patterns (a lithography related effect). A maximum limit on the lateral motion of the junction at the surface, 0.5 micron, can be determined.

To improve resolution the test was repeated using a pattern of 0.125 mm long, parallel, narrow (1 and 2 micron wide) fingers of thermal oxide. After implantation and PEBA, the sample was grooved and stained. The groove was placed at a slight angle to the normal of the lines, insuring that the cut was made through a few patterns. The diffusion of the junction could now be measured using the oxide line width of the same pattern, which reduces lithographic introduced errors. Again, the measured maximum motion of the stained junction was less than 1/4 micron. This experiment was conducted for the liquid-phase pulse anneal at high fluence. If melting does not occur, there is no lateral diffusion.

2.6 ION IMPLANTED PEBA DIODES

2.6.1 Objective

The main goal of this series of experiments was to perform electrical tests on ion implanted, pulsed electron beam annealed junctions. Diode response at both high and low (1 nA/cm^2) currents was measured, as well as minority carrier lifetime and sheet

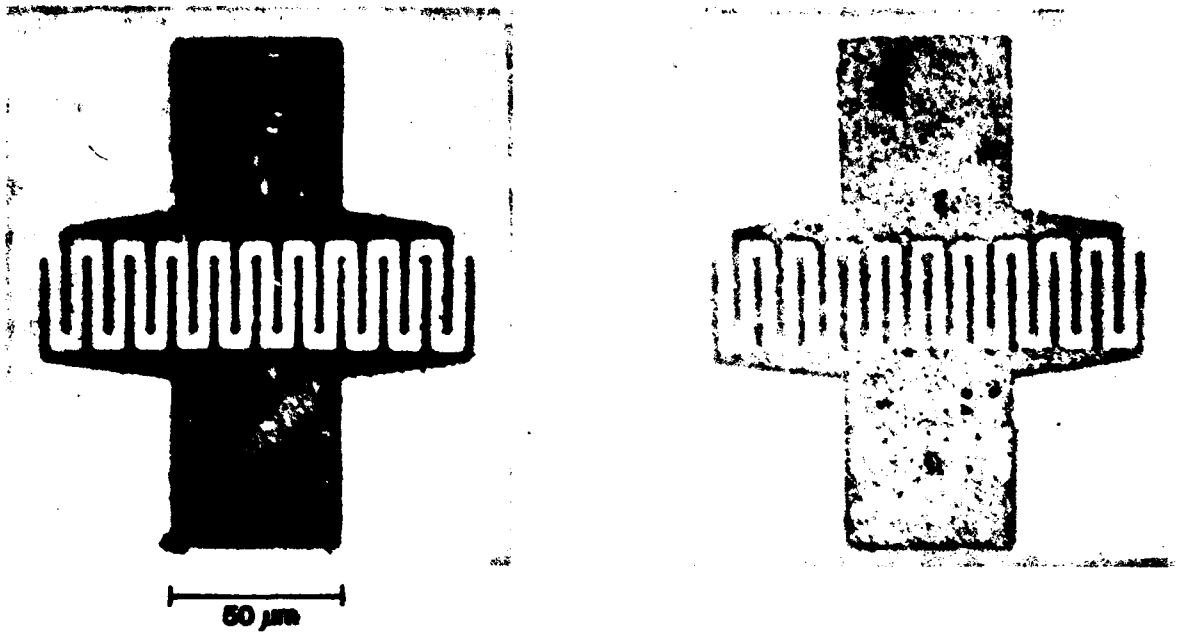


Figure 7. Ion implanted (a) and pulsed electron beam annealed (b) patterns in 0.7 micron thick oxide showing lateral motion of junction was less than 0.5 micron. (Note oxide was removed prior to staining n^+ regions.)

resistance. One series of diodes was examined by DLTS, and an EBIC analysis was performed on a solar cell. Results were compared to similar devices where the implants were annealed in a high temperature (850-950°C) furnace.

A secondary goal of this work was to compare the solid and liquid-phase pulse anneal techniques. This was done for implants at different depths. Also, high dose ion implants which create an amorphous surface layer were compared to less damaging ion implants.

2.6.2 Boron Implanted Diodes

A series of p^+n diodes were fashioned on 4-20 ohm-cm phosphorus doped, (111) silicon wafers. A thermal oxide 0.7 micron thick was grown at 850°C and 100 mil (2.5 mm) dots were etched into it. These samples were then implanted with 10^{15} boron ions/cm^2 at either 25, 50, 100, or 200 keV, followed by a low temperature anneal at 550°C for 60 minutes. The wafers were then split into four groups: (1) no further anneal, (2) 950°C for 15 minutes, (3) PEBA at 1.0 J/cm^2, and (4) PEBA at 0.6 J/cm^2. All samples received a further anneal at 550°C for 60 minutes, 20 mil (0.5 mm) dot contacts on the front and a back contact. This structure has no guard ring.

The sheet resistance for these wafers (Figure 5) was measured by a four-point probe in small rectangles etched into the oxide array from the device structure. Activation of the dopant was discussed in Section 2.5.4. From these data it was surmised that the higher fluence beam did not quite melt the silicon as deep as the tail region (less than 0.3 micron) for the most shallow implant in this series. Also, the low fluence, originally chosen so as to be non-melting, may have melted a very thin layer of silicon approximately 0.1 micron thick. Further interpretation of these data is possible with the additional electrical measurements of these diodes.

The minority carrier lifetime (Figure 8) was measured by the diode reverse recovery technique. The lowest dopant activation and the lowest lifetime measured correspond to the low temperature anneal at 550°C with no other heating. The greatest activation and greatest lifetime were measured for the high temperature anneal, for all implant energies. Results for PEBA are in between these two extremes, with little difference between the values obtained at high or low fluence pulses.

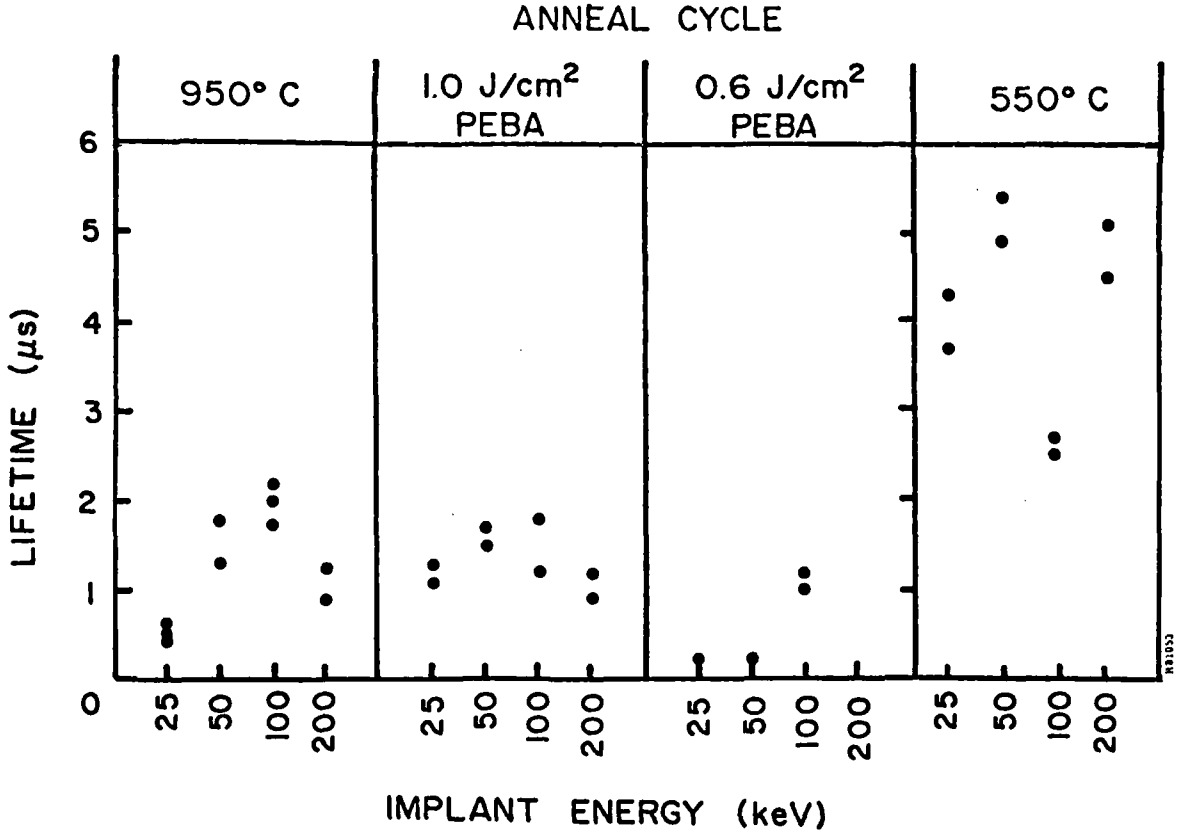


Figure 8. Minority carrier lifetime for p^+n diodes. (Same implant and anneal cycle as in Figure 5.)

The combined data between Figures 5 and 8, suggest that while PEBA may have activated most of the dopant close to the surface and within the melted regions, a significant concentration of defects remain below the melted depth. These defects are probably unannealed damage in the tail of the implant profile.

Low voltage I-V characteristics for these diodes (50 keV implant energy) are shown in Figure 9. Similar curves were obtained for the 25 and 100 keV implants. Low temperature annealed devices had the best ideality factor ($m = 1.08$) and the lowest leakage current (1.1 nA/cm^2 at -0.5 V). The low fluence PEBA annealed devices had similar characteristics. At a higher fluence the leakage current was up to 4 nA/cm^2 with $m = 1.14$. Devices annealed at a high temperature in a furnace had poor characteristics.

The reverse current at high voltage for these devices is shown in Figure 10. Although the breakdown voltage of the diode annealed at 950^{o}C is low, it has a sharp transition. Breakdown characteristics of the low temperature annealed diode are soft. Pulse-processed devices fall in between these two extremes.

The leakage current for all of the devices measured at -0.5 V is shown in Figure 11. The sequence of anneals, 550^{o}C only, PEBA at 0.6 J/cm^2, PEBA at 1.0 J/cm^2, and 950^{o}C anneal, corresponds to ever increasing leakage current for all implant energies. However, the leakage current seems to decrease with increasing ion implant energy for all thermal cycles.

Data in Figures 5, 8, 9, 10 and 11 suggest that the implant damage was more completely annealed by the high temperature, or high fluence pulse; but possible contamination on the wafer surface was driven into the wafer by these processes. The low fluence pulse anneal, which might not have melted the surface, and the low temperature furnace anneal would not have diffused contaminants as far — so some electrical results were better. This is supported to some extent by the lower leakage current for the 200 keV implant. Further characterization of defects was restricted to n^+p diodes.

2.6.3 Phosphorus Implanted Diodes

The device structure was changed for n^+p diodes to include a guard ring, which is required to minimize the effect of inverting a low doped p-type substrate at a thermal oxide interface. The mask set used was designed for JFETs (Section 2.7). The central 200 micron diameter region was implanted with 2.5×10^{15} ions/cm^2 of

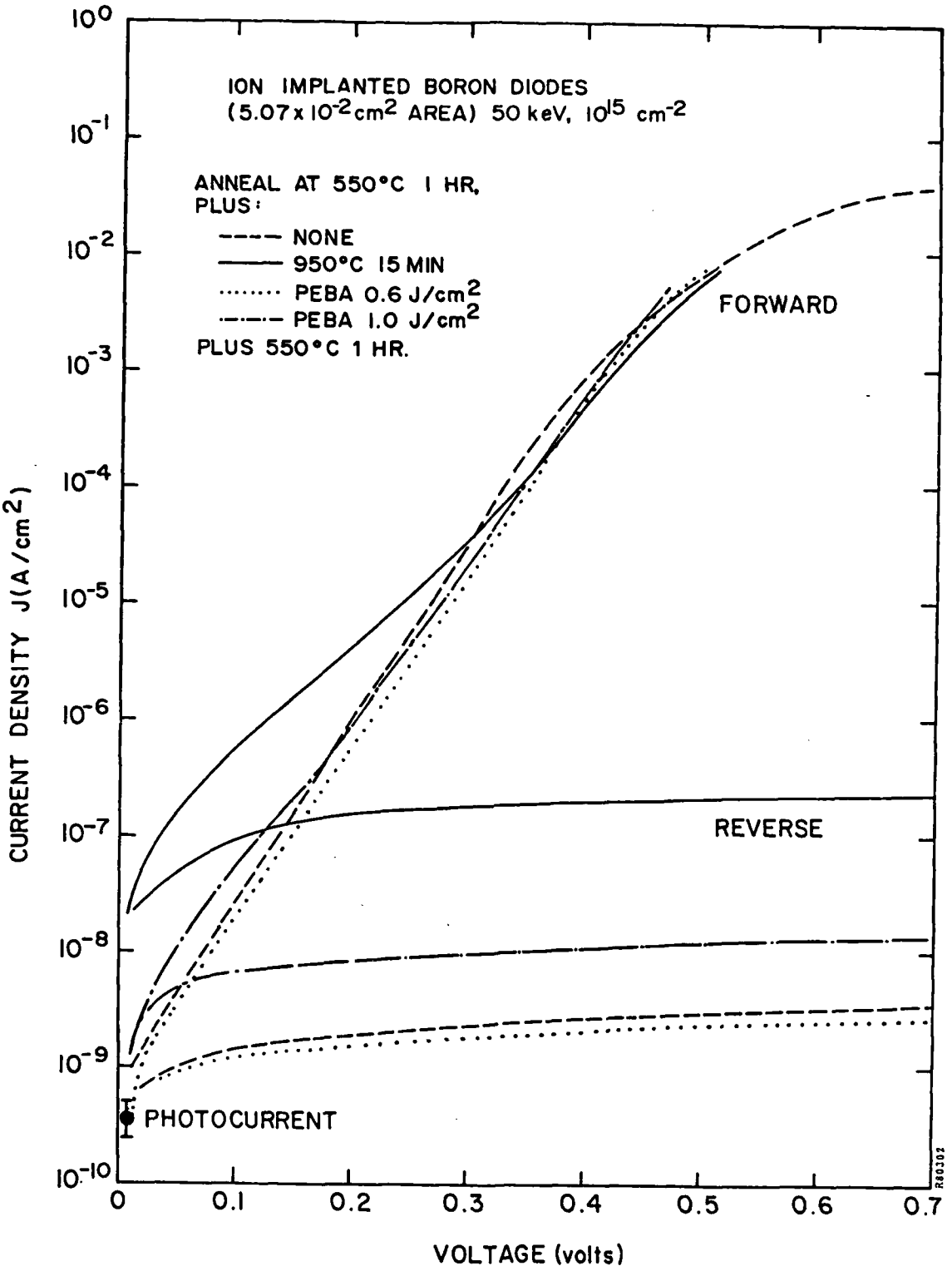


Figure 9. Low voltage I-V curve for p^+n diodes showing low leakage currents and good ideality factors (m) for PEBA processed devices.
(For – – – m = 1.08, ····· m = 1.09, and for –·–·– m = 1.14.)

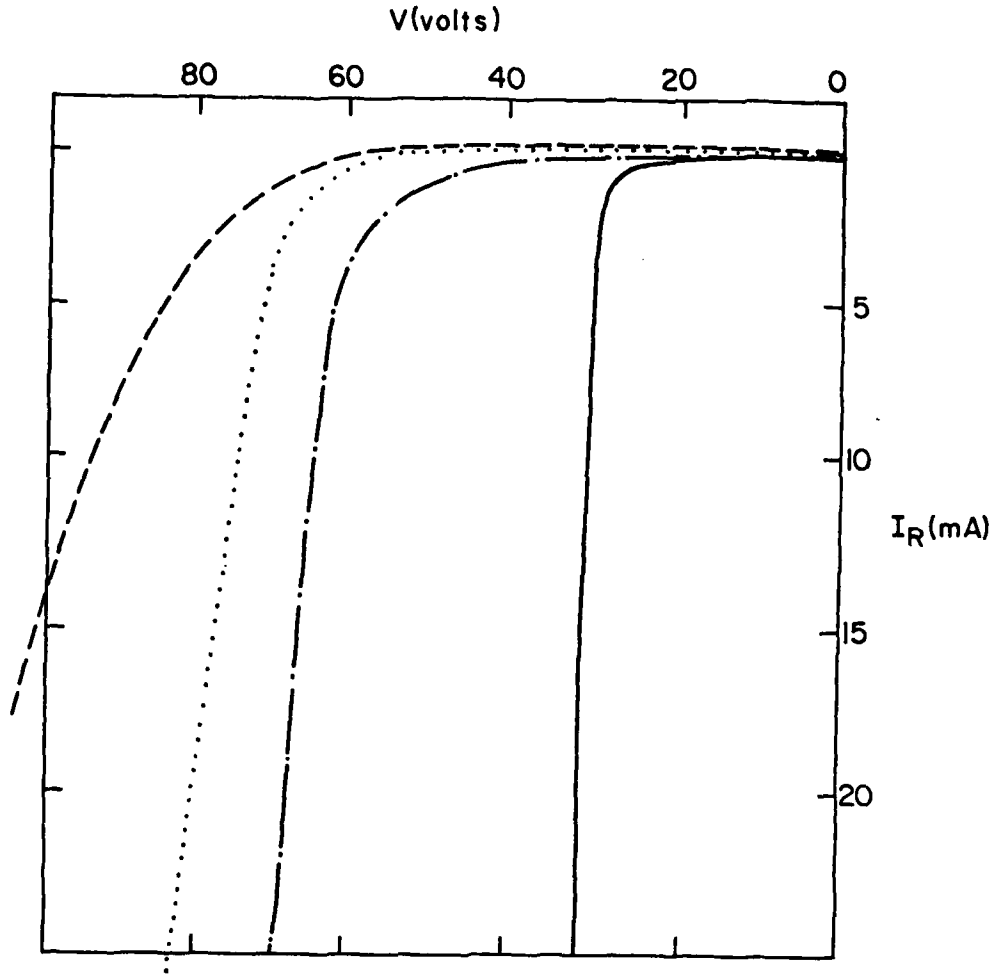


Figure 10. Reverse breakdown characteristics for p^+n diodes comparing PEBA and furnace anneal cycles.

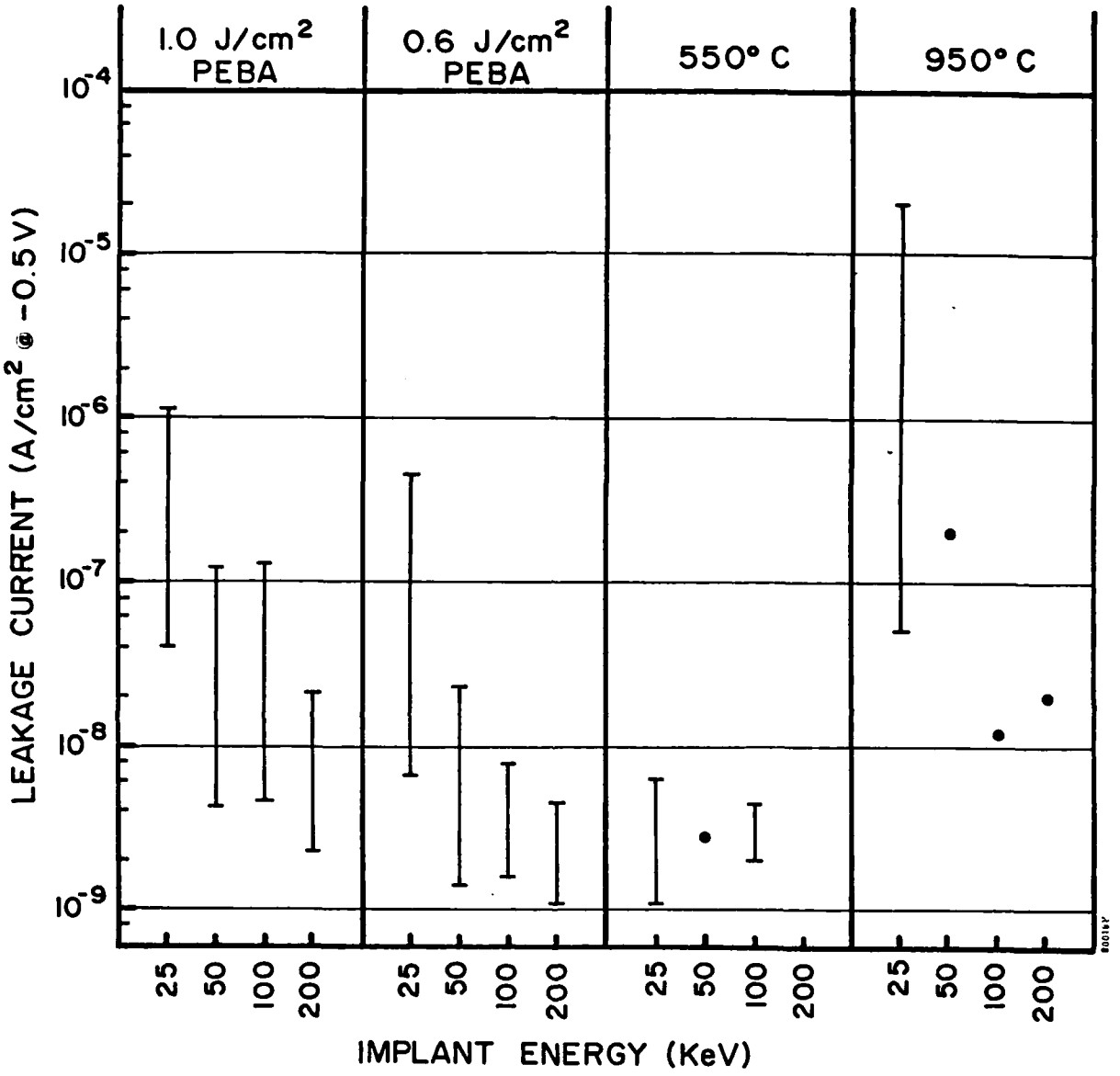


Figure 11. Leakage current for p^+n diodes with 0.05 cm^2 area. Boron implants at 10^{15} ions/cm^2, annealed at 550°C for 1 hour, plus given cycle, plus 550°C for 1 hour.

phosphorus at 10 keV. A 10 micron wide CVD oxide, about 0.3 micron thick, surrounded the central region separating it from the boron-implanted guard ring. Both implants were annealed at the same time. Three annealing procedures were compared including PEBA at 20°C, PEBA at 400°C, and a high-temperature thermal cycle. Pulse fluence was 1.0 J/cm^2. So that fast quenching defects could be examined by DLTS analysis, a low temperature post-pulse thermal cycle was not used. Contacts of Ti-Pd-Ag were applied to the diode, guard ring, and wafer back. Measurements were made through the back contact, leaving the guard ring floating with respect to ground.

The I-V characteristics of these diodes are shown in Figure 12. The melt depth achieved at 1.0J/cm^2 would have been deeper if the surface had remained amorphous, and had not been recrystallized by the low temperature pre-pulse anneal. It is suspected that this would have lowered the leakage current for the pulse annealed diodes (Section 2.5.6), as would have a post-pulse low temperature anneal. These results can be compared to those in Figure 9. The high temperature annealed, phosphorus implanted diode has a much lower leakage current than the corresponding boron-implanted diode.

These diodes were submitted for DLTS analysis.[29] Some peaks in the spectra for pulse annealed diodes were detected, but the signal-to-noise ratio was too small for accurate identification of the trap level. Larger devices were required.

Using the same implant (2.5 x 10^{15} ions/cm^2, $^{31}P^+$ at 10 keV) and substrate (1-2 ohm-cm (100) silicon) as the n^+p diodes, a series of 2 x 2 cm solar cells was fabricated. The implant was annealed by pulsing at 1.0 J/cm^2 at 20°C. No other thermal cycles were used, so that the concentration of "quenched" defects would be enhanced for study. An aluminum alloy back contact was applied before implanting the front surface. Under AM0 illumination these solar cells had an efficiency of 8 percent. With an AR coating and a back surface field (BSF) the expected efficiency would rise to 12 percent. Similar cells, pulse annealed with a post-pulse thermal cycle at 550°C, had efficiencies over 12.5 percent.

After electrical tests, a typical cell was analyzed by EBIC[30], or electron beam induced current imaging in an SEM. The results are shown in Figure 13 at low magnification.

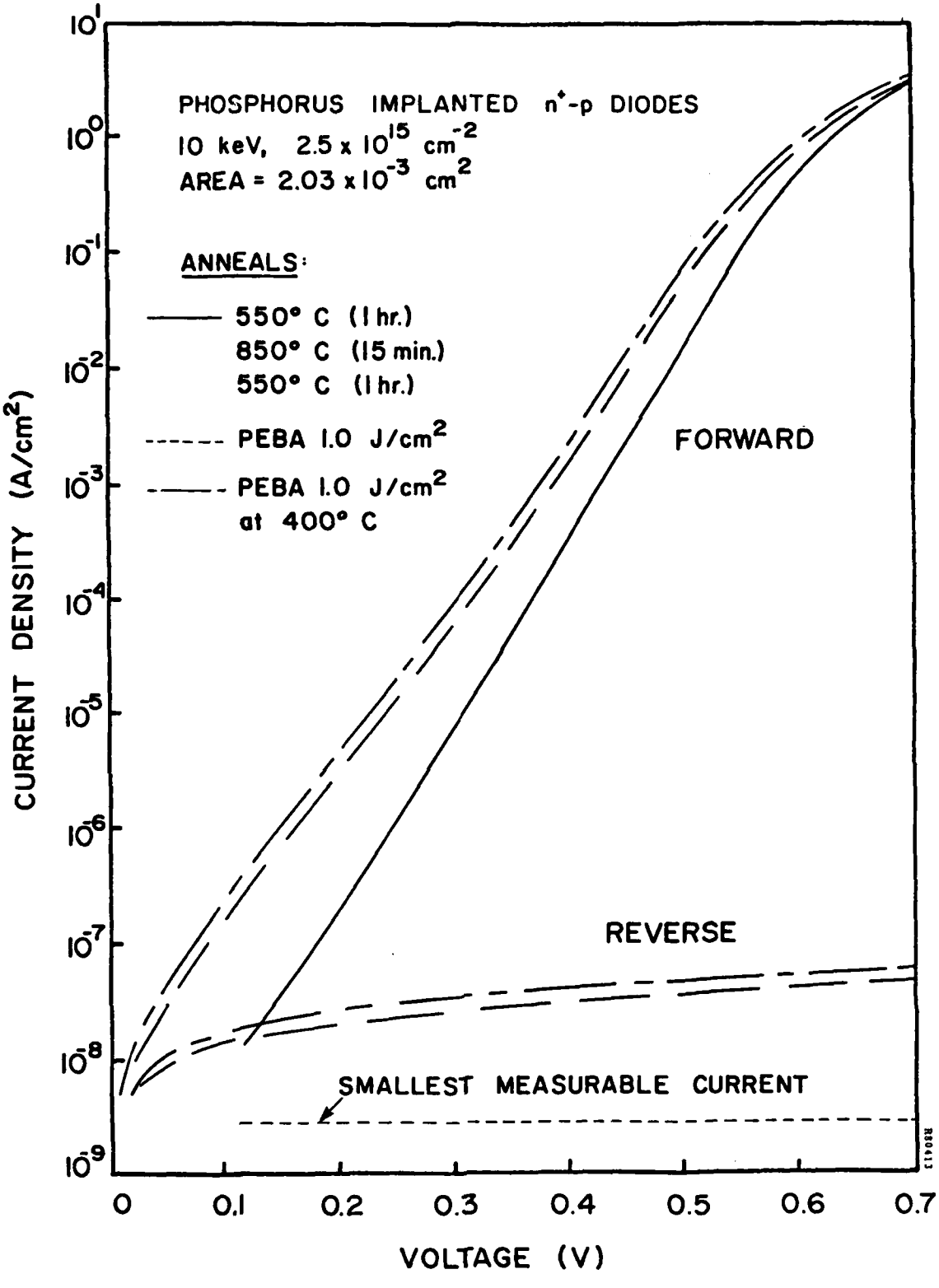


Figure 12. Low voltage I-V characteristics of n^+p diodes comparing PEBA without post-pulse anneal to a thermally annealed device with leakage current less than 2 nA/cm^2.

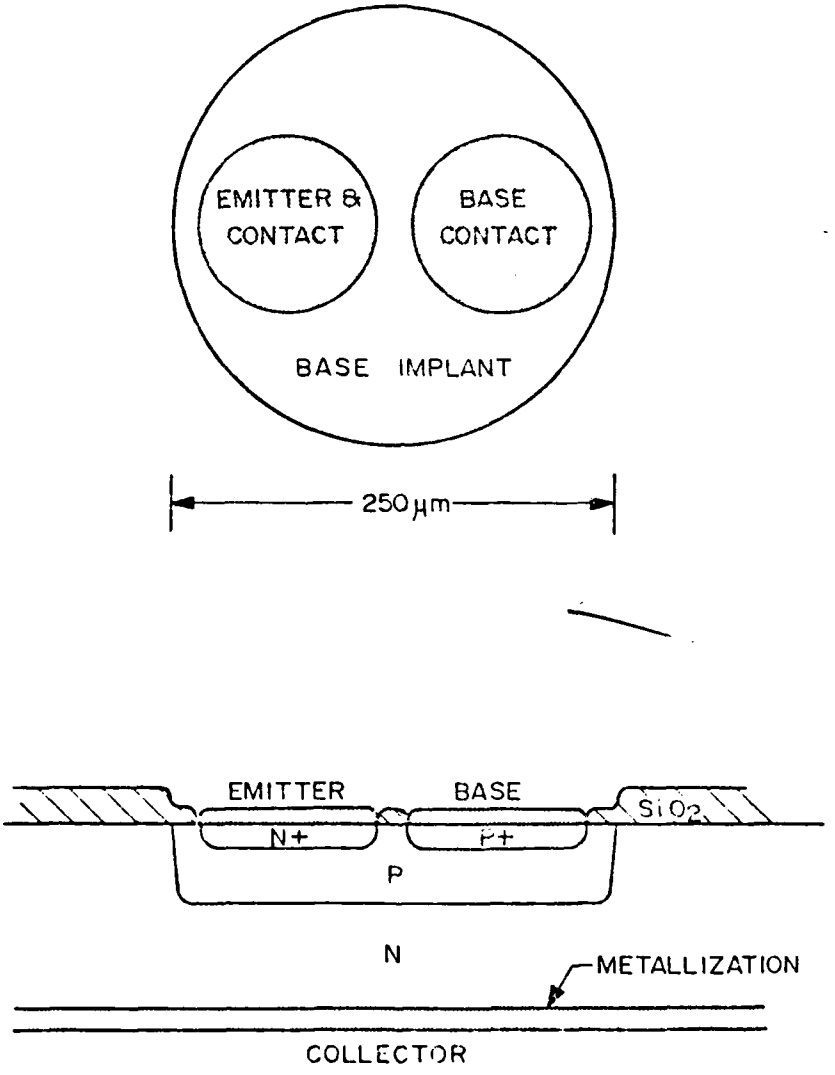
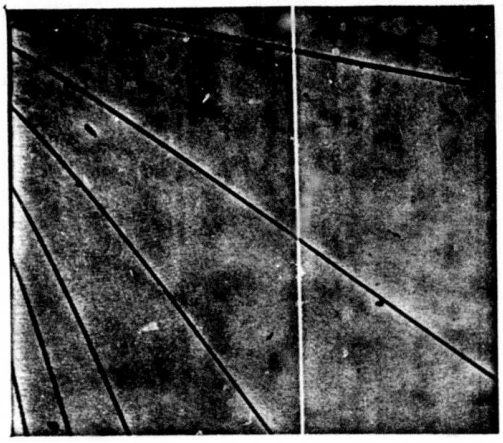


Figure 14. Bipolar transistor structure used to test PEBA process with overlapping.



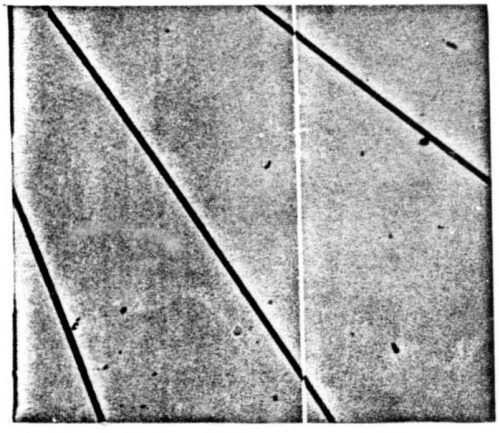


Figure 13. EBIC analysis of n^+p solar cell fabricated by ion implantation and PEBA, showing very shallow defects with pattern related to anode mesh. Bright line scan shows contrast due to 10 percent variation in signal strength.

EBIC analysis gave approximate depth and lateral distribution of residual defects after PEBA. No contrast was visible in the SEM EBIC image for analyzing electron beam energies over 10 keV. This implied that defects were confined, approximately, to the region within one micron of the silicon surface. A speckled pattern with good constrast appeared in the SEM image at electron energies equal to or less than 5 keV. The rough scale of this pattern (1 mm) corresponds to the scale of the mesh anode in the pulse electron beam diode used for annealing. At the higher magnification of 1000x (not shown) there was no variation in contrast of the image at 5 keV. Relative change in silicon signal strength in Figure 13 was 10 percent of the change between the average signal, and the signal from the solar cell contacts. This measurement was made from the line scan incompletely shown.

Interpretation of the lateral pattern implied that there is some shadowing effects in the pulse electron beam from the anode. This presumably can be altered in future tests. Lack of small scale variations in the pattern implied that the pulsed electron beam is otherwise very uniform, with no perturbations other than the 1 mm scale observed.

2.7 ION IMPLANTED PULSE ANNEALED TRANSISTORS

2.7.1 Objective

The goal of this experiment was to test pulse annealing with devices more complex than diodes, and specifically to test PEBA for annealing a shallow implanted junction with a deeper junction present.

Two types of transistors were fabricated by ion implantation and pulsed electron beam annealing through oxide masks. They were low frequency bipolar and JFET designs. Both devices functioned satisfactorily, and had equal gain compared to high temperature, thermally annealed devices.

2.7.2 Bipolar Transistors

Bipolar transistors were fabricated by combining thermal and pulse annealing techniques. The device geometry is shown in Figure 14. The process sequence was (1) growth of a 0.6 micron thermal oxide on an n-type wafer, then etch a region for implanting the base, 80 keV 3×10^{12} $^{11}B/cm^2$, (2) 0.2 micron of spin-on oxide was deposited and densified at $800^{\circ}C$, which annealed the boron implant, (3) an opening (100 micron o.d.) was then etched for the emitter implant of 30 keV, 3×10^{15} $^{75}As^{+}/cm^2$

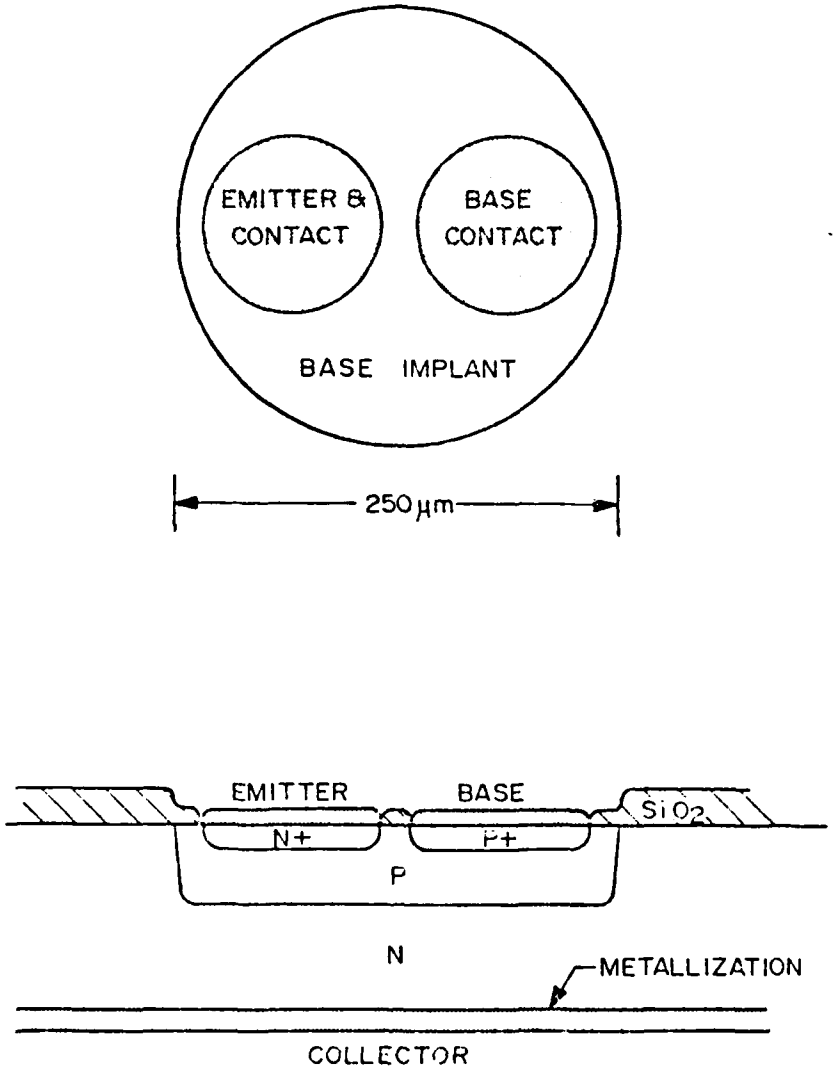


Figure 14. Bipolar transistor structure used to test PEBA process with overlapping.

which was covered with photoresist when a second (100 micron) opening was made for the contact to the base, 40 keV 2×10^{14} $^{11}B^{+}/cm^{2}$. After these steps the wafers were cleaned and given one of the following anneal cycles:

- 550°C 1 hr, PEBA at 1 J/cm^2, 550°C 1 hr
- 550°C 1 hr, PEBA at 1.2 J/cm^2, 550°C 1 hr
- PEBA at 1 J/cm^2, 550°C 1 hr
- PEBA at 1.2 J/cm^2, 550°C 1 hr
- 550°C 1 hr, 950°C 15 min

Contacts were applied, sintered at low temperature, and five devices from each type of anneal were tested.

Test results are shown in Figure 15 for the last two anneal cycles listed above. Pulse annealed devices with the pre-pulse low temperature anneal were non-functional. The gain for devices annealed at 1.0 J/cm^2 was low. The gain for devices annealed at 1.2 J/cm^2 was equal to that of the thermally annealed transistor (about 40). The cause of the low gain at small base currents in the PEBA device is not known.

These results are consistent with previous data. The low temperature pre-anneal was sufficient to regrow the crystal lattice, which changed the amorphous surface of the emitter implant and raised the threshold fluence for annealing. The pulse at 1.0 J/cm^2 should have been sufficient to anneal the arsenic implant, but not the boron contact implant to the base (Section 2.4.4). At the higher fluence, both shallow implants were annealed. Possibly some implant damage remained below the melt depth for the contact implant to the base, contributing to the low gain at low base currents. Note that the low dose, high energy base implant (80 keV boron) was thermally annealed at lower temperatures and longer times than previously used.

2.7.3 JFET

A JFET was designed to test pulse annealing over buried layers. The schematic diagram of the device and characteristic curves are shown in Figure 16. The processing sequence was:

(1) CVD deposition of a 1 micron arsenic doped layer on a 1-2 ohm-cm boron doped substrate

(2) Deposition of 0.3 micron CVD oxide

(3) Etch oxide and implant gate

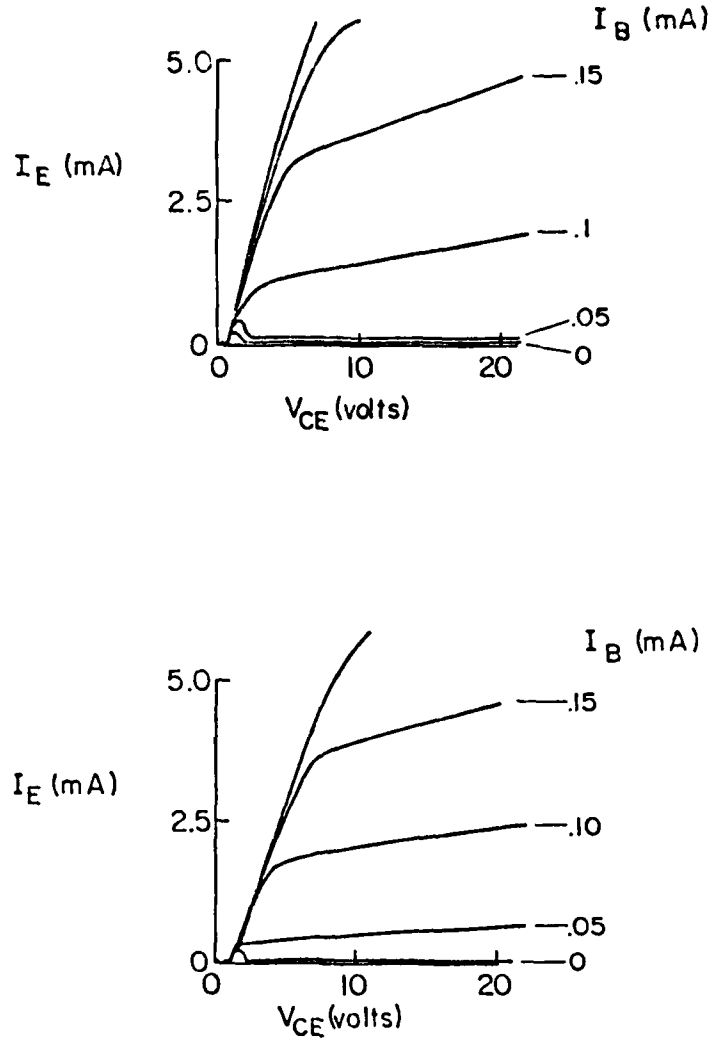


Figure 15. Characteristic I-V curves for npn bipolar transistors comparing PEBA (upper curves) and thermal anneal (lower curves). Note equal gain of 40.

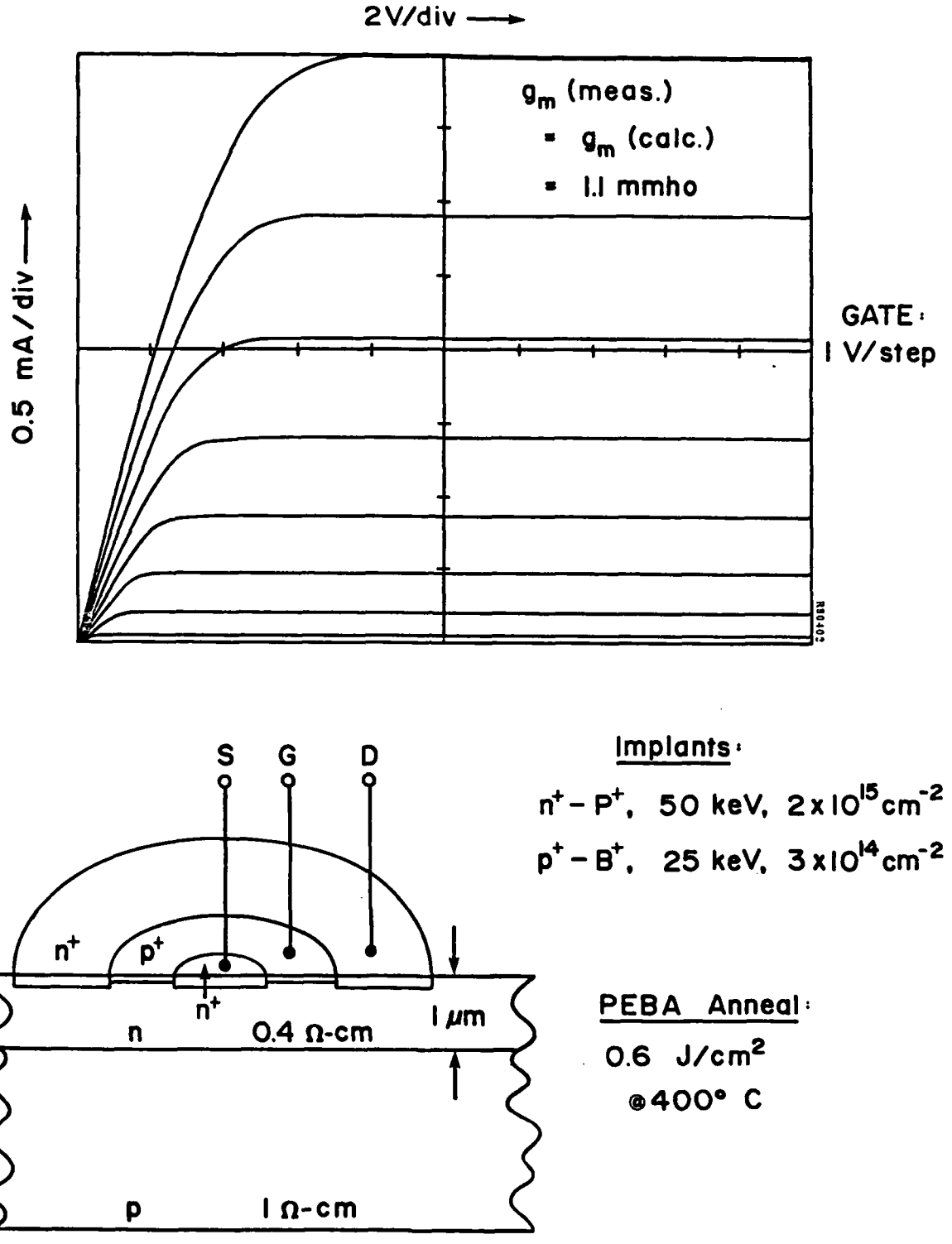


Figure 16. Schematic diagram and electrical characteristics of JFET fashioned by ion implantation and PEBA, showing a gain of 1100.

(4) Etch oxide and implant source and drain

(5) Anneal at either

- 550°C for 2 hours, 950°C for 1 hour
- Pulse at 1.0 J/cm^2 (20°C), 550°C for 1 hour
- Pulse at 0.6 J/cm^2 at 400°C

(6) Evaporate and sinter (400°C) TiPdAg contacts

The lateral dimensions at the JFET were not shown in Figure 16. The outer diameter of the drain was 0.5 mm, and the source, gate, and drain (drawn to scale) were separated by 10 micron wide oxide regions.

The electrical characteristics of transistors annealed by all three types of cycles were similar, with a typical gain over 1000. Reverse didode characteristics for the gate-source region showed slightly increased leakage current and a softer breakdown curve for pulse annealed devices, especially those which did not recieve the 550°C post-pulse anneal. Unannealed damage to the passivating oxide was the probably cause of this leakage.

All low temperature processing was used to fabricate the pulse annealed JFET, except for the epitaxial CVD films, and this step could have been replaced by the pulse epitaxy process discussed in the next section. The one micron deep junction was not affected by PEBA.

2.8 SUMMARY

Pulsed electron beam annealing (PEBA) has been shown to be feasible for annealing patterned ion implanted junctions typical of what can be found in integrated circuit technology. It has been demonstrated that:

- Arsenic, boron, and phosphorus implants can be annealed.
- Implant doses over 10^{13} ions/cm^2 can be annealed.
- Ions implanted as deep as 0.5 micron can be annealed.
- Electrical results as good as thermal anneals were achieved.
- Lateral dopant motion was less than 0.25 micron.
- Vertical dopant redistribution was no greater than 0.3 micron, but PEBA can be used to drive dopants deeper if desired.

- Solid phase activation of implanted dopant by PEBA is possible but incomplete at the pulse width used.
- PEBA is compatible with oxide (over 0.3 micron thick) defined patterns.
- PEBA is uniform on a small scale (less than 100 micron). Observed nonuniformity is attributed to the anode (1 mm scale) pattern, and these variations can be reduced.

As a result of these experiments it was determined that the preferred PEBA process was to heat the sample to 400^{o}C and quickly pulse when hot. An additional post-pulse anneal at low temperatures is desirable, especially if the wafer was covered by passivating oxide films. For ion implants which did not create an amorphous surface layer, the minimal required fluence for the beam parameters used is above 1.2 J/cm^{2}, possible higher. For ion implants which heavily damage the silicon surface, creating an amorphous surface layer, the minimum required fluence was about 1.0 J/cm^{2}. Required fluence increases with the implant depth.

Defects were observed in pulse processed material. They are not identified, but do lie in a very shallow region, in or near the junction depletion region. Some of these defects are believed to be caused by rapid thermal quenching, and are prevented from forming by pulsing heated samples. Most of these defects anneal out at low temperatures (550^{o}C).

SECTION 3
LOW-TEMPERATURE EPITAXIAL FILMS

3.1 DEFINITION OF REQUIREMENT

3.1.1 Objective

The objective of this part of the program was to demonstrate a low-temperature silicon epitaxy process.

The approach was to deposit a polycrystalline or amorphous silicon film on a suitable substrate at a temperature below that required for epitaxial growth. PEBA was then used to melt only the film, restoring single crystal structure to the surface through liquid-phase epitaxy upon cooling. Autodoping and outdoping were precluded, since redistribution of the dopant can occur only in the molten film, not the solid substrate, during the short time scale of pulsed heating.

3.1.2 Epitaxial Layers for VLSI

Parameters for the epitaxial layer desired for integrated circuits depend upon the technology used. For one micron line widths in MOS or conventional bipolar technology, the epitaxial layer is 1 to 3 microns thick with a required dopant uniformity of 30 to 50 percent. For I_2L technology, the dopant uniformity must be better than ± 10 percent in a layer only 0.2 to 1.0 micron thick, depending upon the minimum line width from 0.5 to 1.5 microns.[31] These parameters are within range of the proposed PEBA process.

3.1.3 Effects of High-Temperature Epitaxy

Deposition of epitaxial silicon films on single substrates is easily achieved in the temperature range 950 to 1250°C, but cannot be achieved at low temperatures. There is some plastic distortion of the silicon wafers at these high temperatures,[3] which is not critical until submicron geometries are used for integrated circuits.

More important is the problem of autodoping,[32] or the transfer of dopant from one part of the substrate to another. For integrated circuits, the epitaxial layer of silicon will typically be deposited over a substrate with a patterned buried layer (e.g., n^{++} on a p-type substrate). Autodoping causes changes in this pattern, so that the resolution of this pattern and the thickness of the epitaxial layer are limited to insure isolation.

One source of autodoping, transfer of the dopant from the wafer into the gas stream and back, is reduced at low pressure. Another source of autodoping is the diffusion of the dopant from the substrate into the growing epitaxial layer, both laterally and vertically. Presently, this can only be controlled by using dopants with low-diffusion coefficients (such as arsenic) and by growing the epitaxial film rapidly so that the film thickness, and space between buried pattern lines, is much greater than the mean diffusion distance.

3.1.4 Advantages of PEBA

Autodoping is the problem most effectively reduced by pulsed electron beam liquid-epitaxial regrowth of low-temperature deposited films. If the deposited film does not have to be epitaxial as-deposited, then a parameter regime for chemical vapor deposition (CVD) can be used to put down very pure, undoped silicon films at temperatures which preclude diffusion of dopants. Extremely sharp stepped dopant profiles were achieved in this program. Autodoping did not occur.

By accurately controlling the melt depth of the PEBA process, the deposited film can be melted to the original substrate interface. This has been achieved with amorphous films.[15] Dopant in the solid substrate cannot diffuse a significant distance during the time (less than 10 microseconds) that the surface remains at high temperatures, although dopant in the molten material is rapidly redistributed. This separation of dopant between film and substrate precludes autodoping during epitaxial regrowth of the film.

The proposed process can have the high throughput required for production applications. PEBA is a vacuum process and contaminants are not introduced during melt. High-quality films are possible.

3.2 MODEL OF PULSED EPITAXIAL REGROWTH

3.2.1 Overview

The model for pulsed electron beam liquid epitaxy of a deposited film is identical to the melt model for PEBA annealing of an implanted layer. Referring to the schematic diagram in Figure 1, replace implanted layer by deposited layer, and the temperature profiles for either case are the same. This holds, provided both surfaces are polycrystalline or both are amorphous.

Two changes are made for the epitaxy of a deposited film. First, the film thickness desired is greater than the junction depth for most implants. To avoid surface damage (Section 2.4) when melting, the thicker silicon layer requires a change in electron beam parameters.

Second, the interface between the deposited film and the substrate is critical for epitaxy. Silicon-oxide or SiO_2 molecules in a thin residual layer at this interface diffuse slowly in molten silicon. Epitaxial growth cannot occur if the oxide layer is present and continuous. Either the surface must be melted to a depth beyond the original interface — so that the oxide molecules can diffuse in the melt and liquid epitaxy can occur — or the oxide layer must be removed before film deposition. Removal of the oxide layer is preferred, but difficult at low temperatures.

3.2.2 Model of Energy Deposition

The electron energy deposition profile must be determined for a given process to achieve the correct melt depth and to maintain the surface temperature history within prescribed limits. These limits are the melt temperature ($1410^{o}C$) and the vaporization temperature ($2355^{o}C$). The electron beam used for annealing ion implants cannot melt a layer of silicon deeper than approximately 0.5 micron without causing surface damage. To melt deeper layers, new electron beam parameters had to be developed for the PEBA epitaxy process. The average angle of incidence of the electron beam upon the sample was changed, to reduce the slope of the energy deposition profile near the surface (Figure 17). This reduced the thermal gradient and the thermal stress, which initiated damage through slip or vaporization of the silicon. With a higher fluence threshold for damage, a thicker silicon film could be melted.

3.2.3 Model of Melt Depth Versus Fluence

Control of melt depth is more critical for the pulsed-epitaxy process than for the pulsed-annealing process. The entire deposited film must be melted for epitaxy. The increase in melt depth beyond the film-substrate interface determines the amount of dopant from the buried layers that will appear in the film. Isolation requires minimizing this variation in melt depth below the interface.

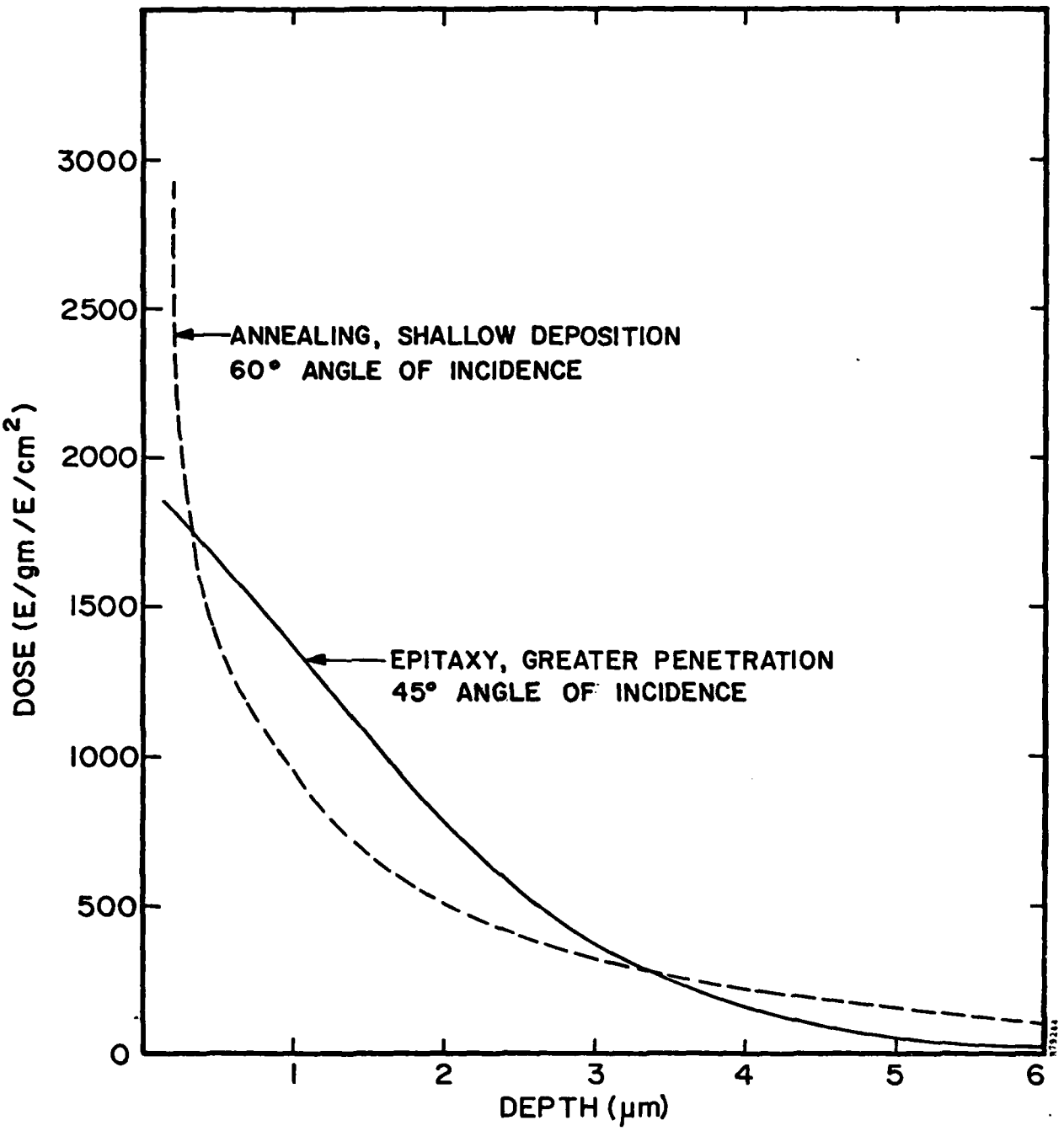


Figure 17. Depth dose profiles in silicon for two electron beams adjusted for annealing (shallow heating) or epitaxy (deeper heating).

The thermal model presented in Section 2.3 was suited for predicating the minimum fluence required to melt the entire implantation damaged surface layer. In that model the melting temperature of amorphous silicon was assumed to be 1410°C, while the heat of fusion was reduced from that of crystalline silicon. The model is consistent with the film recrystallizing while it is being heated by the fast energy pulse. Because the melt temperature of the substrate and film were assumed equal, this model predicts a smooth transition in melt depth as a function of fluence. This is shown in Figure 18, after Baeri et al.[15]

A further consideration is that the amorphous-silicon film may not recrystallize as it is being heated, and may melt at a lower temperature than that of crystalline silicon.[14] This is conceivable because the melt front velocity upon heating is so high (Section 2.3.3). Using the appropriate electron beam parameters for pulsed epitaxy, new calculations show a sharp discontinuity in melt depth as a function of fluence when a varying melt temperature is taken into account.[15] This is shown as a dotted line in Figure 18. This effect, if present, would allow accurate control of the melt depth to the film-substrate interface.

3.2.4 Model of Dopant Diffusion

Diffusion of dopants during pulsed liquid-phase epitaxy (LPE) is much different than in conventional chemical vapor deposition (CVD) epitaxy. Outdiffusion of dopant from the substrate into the film follows an error function profile in CVD epitaxy,[33] whereas an exponential profile is expected from LPE. Figure 19 shows exponential type curves which are the result of a numerical, finite element approximation to solve the diffusion equation. This model assumes that:

(i) The deposited polycrystalline or amorphous film is undoped,

(ii) The substrate is uniformly arsenic doped to 10^{19} atoms/cm^3 initially,

(iii) The interface is perfectly sharp initially,

(iv) At t=0 (initial condition) the deposited film plus a fraction of the substrate equal to one-tenth the thickness of the film is melted,

(v) The liquid-solid interface moves toward the surface at a constant velocity of 0.5 m/s (Section 2.3) when cooling, and

(vi) The diffusion coefficient in the liquid phase is 3.4×10^{-4} cm^2/s and zero in the solid phase.

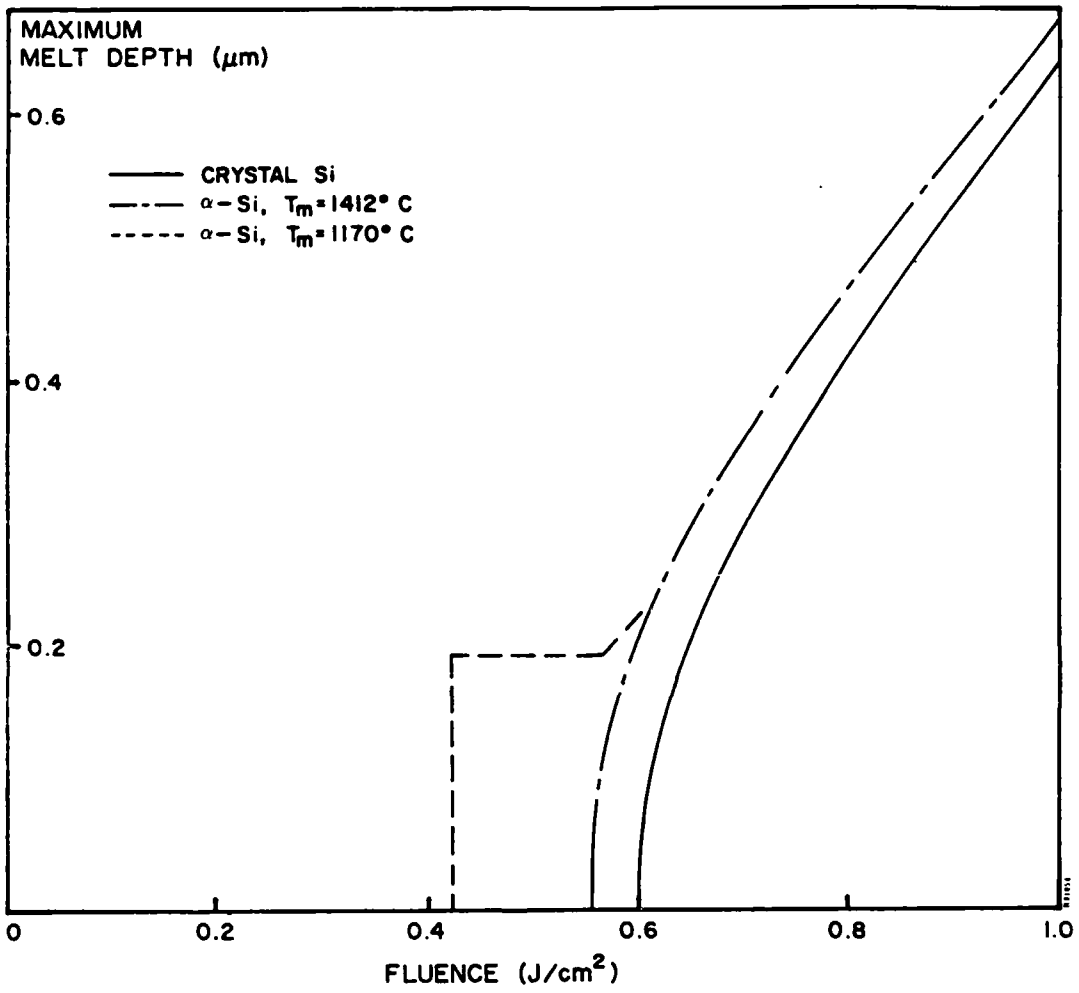


Figure 18. Calculated maximum melt depth as a function of electron beam fluence for crystal silicon, and same covered with 0.19 micron thick amorphous silicon (α-Si) film. Enthalpy of melting α-Si taken as 1220 J/g, compared to 1790 J/g for crystal Si, after reference 15.

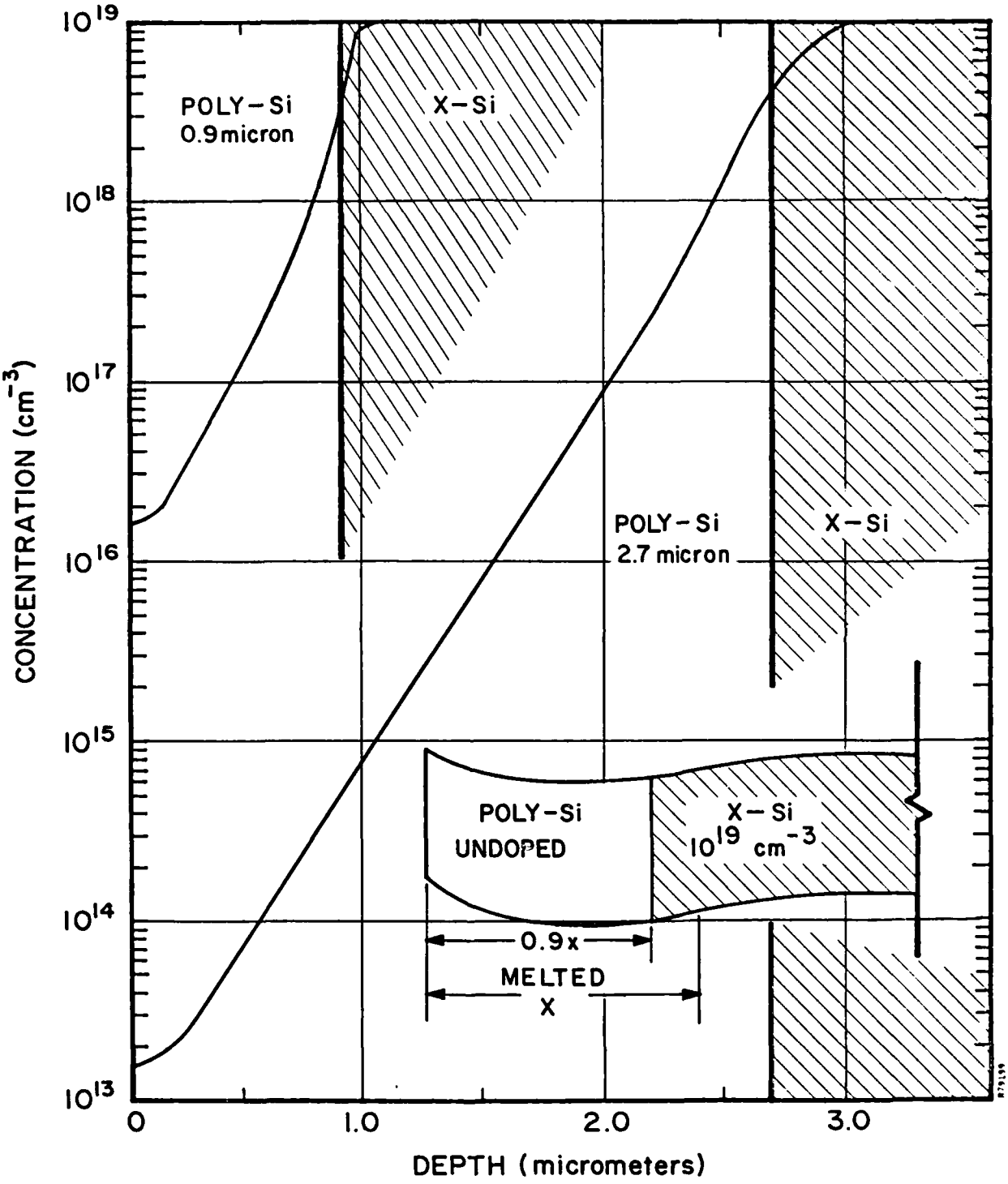


Figure 19. Calculated diffusion of dopant from a substrate into pulsed electron beam liquid-phase epitaxially regrown films, when the film thickness is 90 percent of the melt depth.

This model is not exact in that it does not accurately reflect temperature changes in the molten region as a function of time. However, the motion of the liquid-solid interface agrees reasonably well with more accurate time-varying temperature calculations. Also, changes in the liquid-diffusion coefficient with temperature are not important, since the temperature of the molten region is nearly constant when cooling. Lateral diffusion of the dopant was not modeled.

3.3 LPCVD Films

Two vendors were used for low-pressure chemical vapor deposited (LPCVD) polycrystalline and amorphous films. It is believed that slightly different methods of inserting the substrates into the reactor led to different oxide thicknesses on the surface prior to deposition. Since this residual oxide film was not etched in situ, the change in surface oxide led to different results for pulsed samples. Original, as-deposited films were similar.

3.3.1 Deposition and Pulse Processing

The first set of LPCVD films[31] was deposited upon 2-inch substrates, from silane at 0.255 torr, at a temperature between 605°C and 628°C. The deposition rate was 8.5 nm/s. Average total thickness of the film was 0.4 micron, with a wafer-to-wafer variation of ±20 nm and a uniformity on a wafer of ±3 percent. Two different substrates with (111) orientation were used; 0.003 ohm-cm arsenic-doped silicon, and 0.02 ohm-cm antimony-doped silicon. Dopant was not added to the gas stream during deposition. Nominal dopant concentration in the film was about 10^{15} atoms/cm^3 due to autodoping effects. After deposition there was a slight haze on the wafers, with an operator's comment that he thought the cleaning was less than satisfactory.

These films were deposited without completely etching the oxide surface layer on the substrate. Wafers were cleaned in HF before insertion into the reactor. However, because the substrates were heated prior to insertion into the vacuum vessel, the surface oxide thickness was approximately 4 nm. Complete removal of this oxide film in the reactor is possible, but requires etching at 1175°C in HCl, which is contrary to the low-temperature processing desired.

PEBA processing of these samples used the alternate electron beam parameters described in Section 3.2.2. The average particle energy was 12 keV and the average angle of incidence was 45^{o}, resulting in the energy deposition profile of Figure 17. The total fluence was varied from 0.9 to 1.8 J/cm^2, but the value used for the analyzed results reported was 1.1 J/cm^2. Pulse width was 100 ns, and the sample temperature was always 20^{o}C. The beam diameter at the sample was reduced to 1 cm for characterization studies.

3.3.2 Crystal Structure

These films were analyzed by reflected high-energy electron diffraction (RHEED) and electron channeling to determine crystal structure.[32]

RHEED patterns shown in Figure 20 were generated on a TEM at 100 keV with the electron beam at a glancing angle to the surface. This technique is only sensitive to the top 10 nm of the silicon sample, and therefore separates the structure of the film from that of the substrate. In Figure 20 the structure of the as-deposited films before pulsing shows a small-grain (less than 0.1 micron), randomly oriented polycrystalline silicon layer. All of the ring spacings can be identified with silicon; no contaminants were detected. After pulsing at over 1.1 J/cm^2 the pattern changed, showing strong Kikuchi lines characteristic of a single crystal with long-range order. Samples pulsed at a lower fluence, below 0.9 J/cm^2, did not show this change.

Electron channeling patterns (TEM) of the as-deposited films were uniformly gray and without contrast. The patterns were similar to those obtained from a 50 nm evaporated amorphous silicon film on a single-crystal substrate. After pulsing the channeling pattern reverted to that of the single-crystal substrate.

These data were interpreted as proving good-quality epitaxial regrowth of the deposited film occurred as a result of PEBA processing. Dopant profiles discussed in the next section proved that the film did not blow off the substrate, and that this analysis was of the film structure.

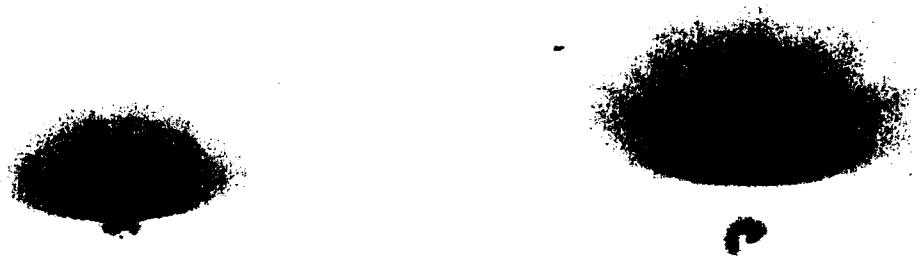


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Figure 20. RHEED patterns of 0.4 micron LPCVD polysilicon film before and after pulsed electron beam irradiation, showing a change in microstructure from small-grain random polycrystalline material to a single crystal structure with epitaxial orientation.

3.3.3 Composition Analysis

The arsenic-concentration profiles for the as-deposited and pulse-processed films are shown in Figure 21, along with the calculated dopant profile (after Figure 19) and the profile in a CVD epitaxy film. Measured data were scaled from SIMS analysis which originally gave detected dopant as a function of sputtering time. An approximate depth scale was fitted to that data based upon the crater depth at the end of the analysis and assuming a constant sputtering rate. The scale for arsenic concentration was fixed by resistivity measurements of the substrate, giving a concentration of 2×10^{19} atoms/cm^3 in the original wafer.

The As-deposited film has a very abrupt nn^+ junction, less than 50 nm. The data in Figure 21 may have been broadened by the measurement technique. After pulsing, the dopant profile follows the calculated value, which implies liquid-phase epitaxy as opposed to solid-state diffusion of the dopant and also implies an average melt depth of about 0.45 micron. The CVD profile shown is from an error function calculation for deposition at about 1 micron/min at 1050°C.[33]

Concentration profiles for the contaminants oxygen, carbon, nitrogen, and hydrogen are shown in Figure 22. The arsenic profile shown was the original data, replotted in Figure 21. Neither the absolute nor relative concentration of the contaminants can be inferred from this SIMS data, since the sensitivity of the instrument varies for each ion and is not calibrated. The signal for hydrogen is noisy and not useful. The signal for nitrogen is actually a plot of SiN to enhance detection limits. The increase in all signal levels near the surface is caused by the native oxide layer and a change in the sputtering rate through this thin film.

The data in Figure 22 can be used to compare contaminant levels in the deposited film and substrate, and to show profile changes after pulse processing. Oxygen and nitrogen concentrations in the film and substrate are nearly identical. However, the carbon concentration in the deposited film is a factor of 4 to 5 higher than in the substrate. The level of all contaminants is enhanced at the original film-substrate interface where the unetched oxide layer is clearly visible. The thickness of this interface is broadened by the slow sputtering rate of SiO_2 (a factor of 6 to 10 times slower than silicon), and a non-uniform sputter crater depth (± 5 nm at the end of the analysis).

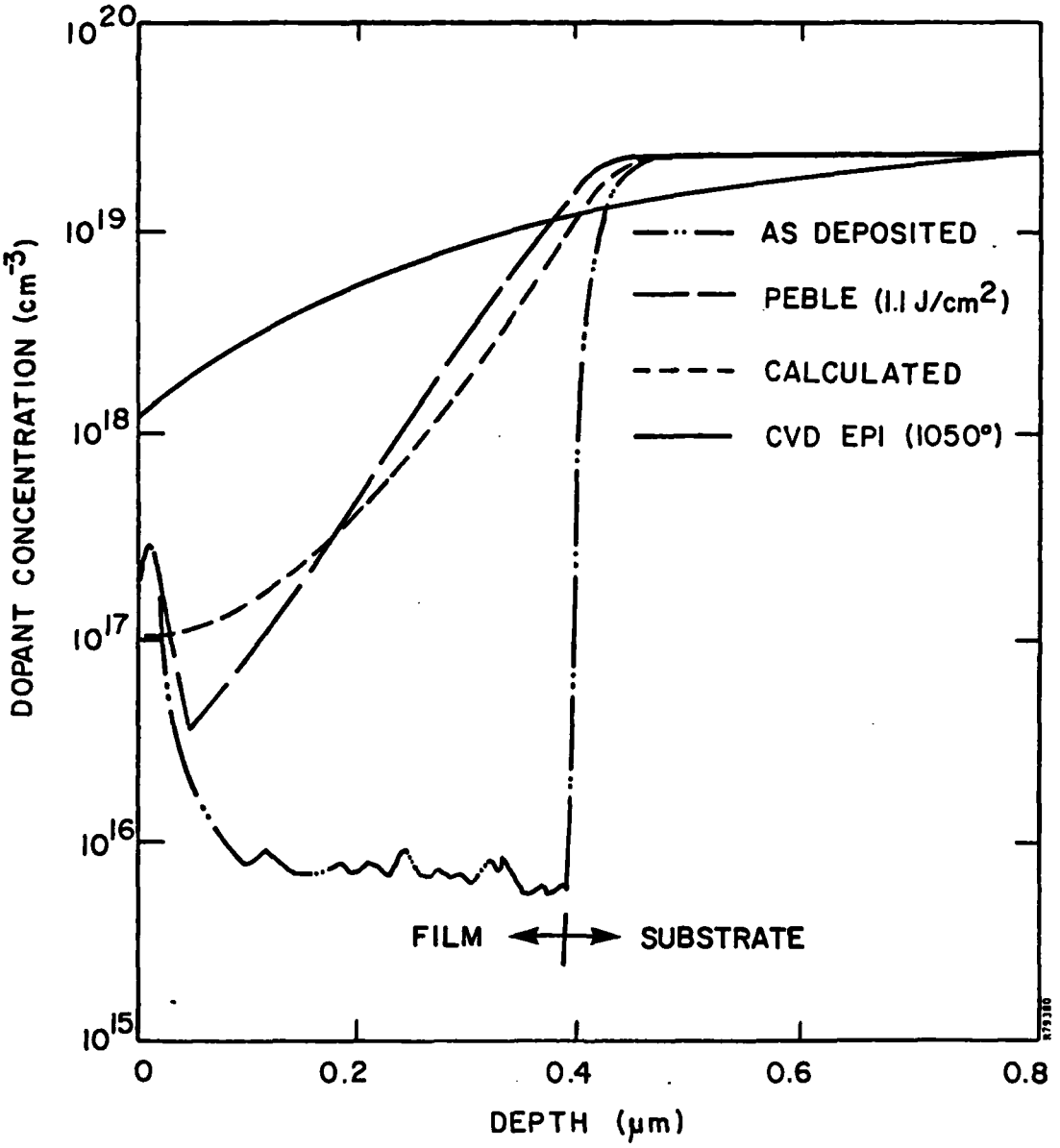

Figure 21. Dopant (arsenic) concentration profiles measured by SIMS in as-deposited LPCVD films, and in the same film after PEBLE, showing correlation to calculated values from Figure 9.

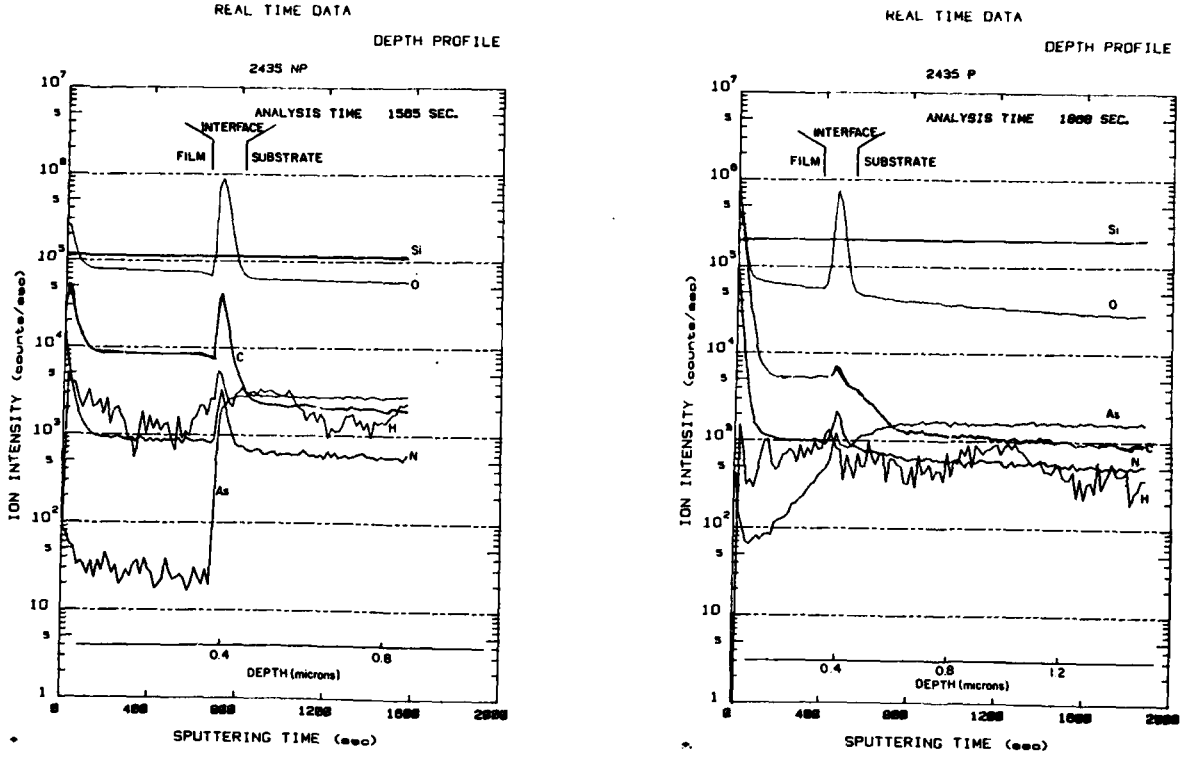

Figure 22. SIMS[24] profile of As, C, H, N, and O before and after pulsing 0.4 micron LPCVD polysilicon film (Figure 20) showing the diffusion of As, C, and N and the increased concentration of impurities at the interface. Note that oxygen did not diffuse away from the 40 nm interface broadened by the measurement technique.

After PEBA, the arsenic and carbon profiles show clear changes from the original step-function distribution. Effects of liquid-phase epitaxy for the case of a higher dopant concentration in the film can be inferred from the carbon profile. The implied melt depth is about 0.6 micron. The SiN profile shows a change in that the height of the peak concentration at the original film-substrate interface was reduced after pulsing, implying that some of the nitrogen diffused at least 250 nm.

By comparison, the oxygen peak shows no reduction, implying minimal diffusion for oxygen atoms or the SiO and SiO_2 complexes to which they may be tied. Since epitaxial growth of the film was observed, the SiO_2 layer could not have remained continuous. Holes must have appeared in the layer through which crystal growth proceeded rapidly, spreading laterally on top of the oxide film.

3.3.4 Electrical Characterisitcs

A C-V profile of the carrier concentration for the pulsed epitaxy layers on antimony doped substrates closely followed the exponential dopant profile expected from calculations similar to those in Figure 9.

3.3.5 Other LPCVD Films

A second lot of LPCVD films[34] was deposited upon (100), 10 ohm-cm silicon wafers. Some of the substrates in this lot had a shallow ion-implanted junction of arsenic which was annealed by either PEBA or a high temperature furnace anneal. Half of the films were deposited at 625°C and half of the films were deposited at 550°C. Other deposition conditions were similar to those described in Section 3.3.1.

The films deposited at lower temperatures were amorphous as determined by ellipsometric analysis.[34] However, RHEED analysis showed a fine-grain polycrystalline structure, similar to that in Figure 20. The source of the discrepancy is uncertain, but the amorphous films were unstable and the analysis occurred a few weeks after deposition.

These films were not epitaxial after pulse processing over a range of fluence from melt to damage threshold. Neither the amorphous nor polycrystalline films, on either the bare substrate or over the n^+p diodes, would convert to epitaxial films. Some samples were implanted with silicon at 25 keV to a dose of 5×10^{15} ions/cm^2 to insure an amorphous surface layer; they would not convert to epitaxial films either.

SIMS analysis of the as-deposited films showed an increase in oxygen concentration and an increase in the width of the peak at the film-substrate interface compared to Figure 22. It is believed that slightly varying sample handling procedures increased the thickness of the native oxide layer for these samples relative to the first set. This oxide film apparently remained continuous, even though the PEBA process melted silicon on both sides of the interface, and prevented epitaxial growth of the film.

3.4 CVD EPITAXIAL FILMS

3.4.1 Deposition

Two types of CVD films were deposited. Polycrystalline layers were used as samples for PEBA epitaxy. CVD epitaxial layers were used for comparison of structure, composition, and electrical properties.

Epitaxial films were deposited at atmospheric pressure in conventional induction heated horizontal (Model AMH-630) or vertical pancake reactors (Model AMV-800).[31] Dopant was not added to the gas stream; however, residual dopant (arsenic) from the regular use of these reactors, plus autodoping effects, was sufficient to make all films less than or equal to 1 ohm-cm resistivity, n-type. Prior to epitaxial film growth, the 1.5 to 2.0 nm native oxide layer was etched off the substrates by HCl at 1200°C in two minutes in situ. After purging, films were deposited from silane (SiH_4) diluted in hydrogen at 1050°C, or from $SiCl_4$ at 1150°C. Growth rates were approximately 0.5 micron/minute and 1.0 micron/minute, respectively.

Highly doped substrates (about 10^{19} atoms/cm^3) were chosen for all initial experiments. This combination produced measurable vertical dopant profiles (for SIMS analysis), with minimal sample preparation, applicable to the problem of depositing an epitaxial film over a buried layer. Also, an nn^+ film-substrate with a shallow, very sharp junction would have immediate applications to microwave devices.

3.4.2 Composition

Dopant profiles for two, as-deposited thin layer epitaxial films are shown in Figures 23 and 24. The first film was deposited from silane and the arsenic concentration profile from SIMS measurements is compared to the carrier concentration from a C-V profile in Figure 23. The second film was deposited from $SiCl_4$, and the SIMS profile for arsenic as well as the contaminants oxygen, hydrogen, carbon, and nitrogen are shown in Figure 24.

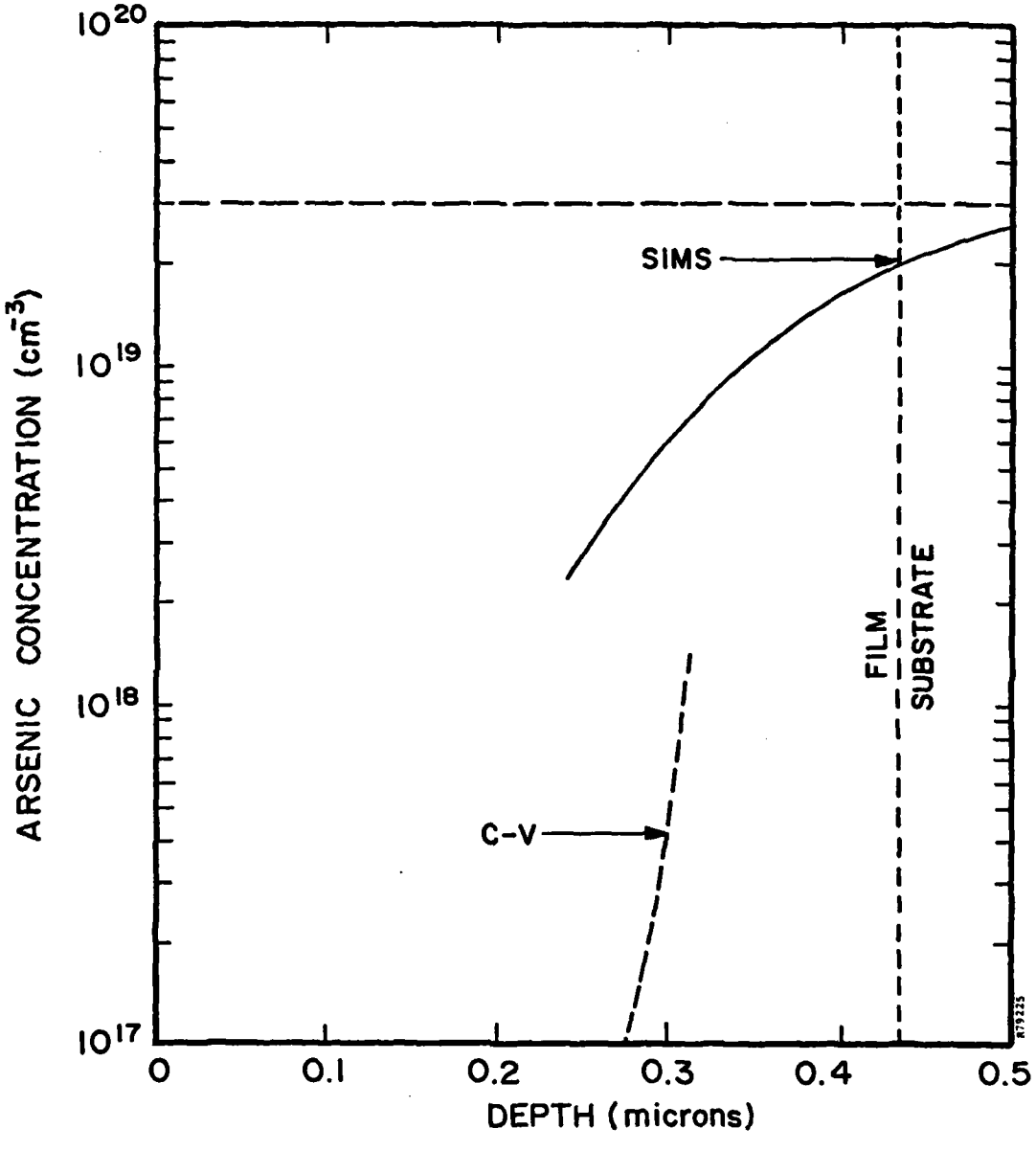

Figure 23. Dopant profile in epitaxial CVD silicon layer (deposited from silane at 1050°C) as measured by secondary ion mass spectroscopy (SIMS) and capacitance-voltage curves.

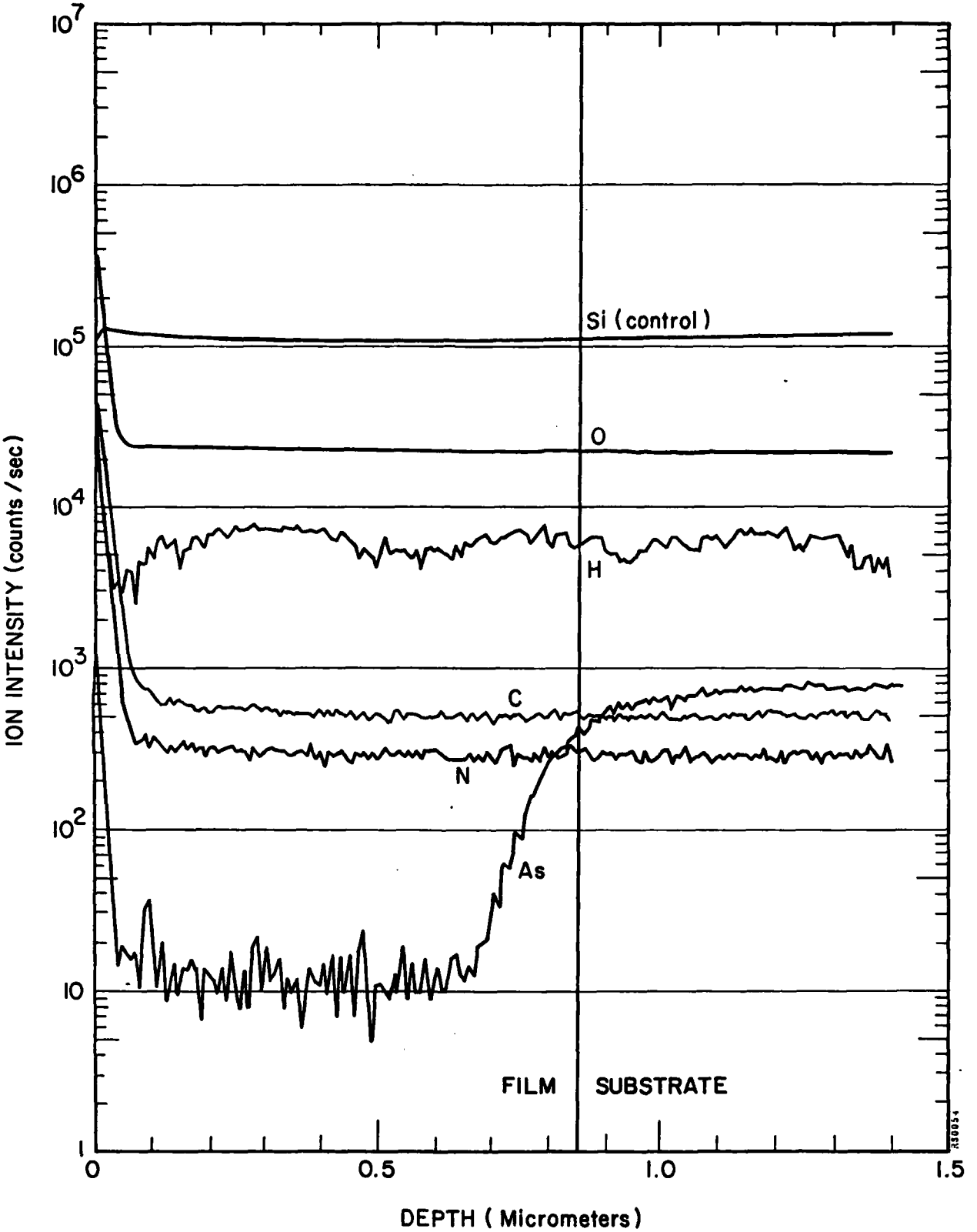

Figure 24. Dopant and contaminant profiles in an epitaxial CVD silicon layer deposited from $SiCl_4$ at 1150°C on a 0.003 ohm-cm arsenic doped substrate. This is the sharpest junction profile which can be obtained by conventional CVD epitaxy.

The calibration for the arsenic concentration was determined from the measured resistivity of the substrate (0.003 ohm-cm). In both cases (Figures 23 and 24), the arsenic concentration increases from the minimal detection limit of the equipment in the film, to the background substrate doping at a narrow interface 200 to 300 nm wide. This width is much greater than that shown in Figures 21 and 22 for LPCVD films. However, for CVD epitaxial films they are considered very sharp junctions with minimal autodoping, equal to the state of the art.

In Figure 24, the contaminant profiles for oxygen, hydrogen, nitrogen and carbon are flat except for the thin surface layer. There is no change between the film and the substrate, compared to variations shown in LPCVD in Figure 22. Although the absolute concentration of these contaminants cannot be inferred from this data, the background levels for detecting carbon and oxygen on this modified equipment[24] is below 10^{17} atoms/cm^3. From estimated noise levels, the oxygen concentration clearly exceeds this limit, while the carbon concentration remains uncertain.

3.4.3 Structure

A series of epitaxial films, nominally 0.2, 0.5, 1.0, and 3.0 microns thick, was deposited from silane on (111) arsenic doped (0.003 ohm-cm) substrates. Samples were submitted for structural analysis by TEM. Electron channeling patterns from the four films and a typical single-crystal substrate were identical. RHEED patterns from the thinnest film, and from a typical single-crystal substrate, were also identical and resembled the good pattern shown in Figure 20 for a converted LPCVD film.

3.5 CVD Polycrystalline Films

3.5.1 Deposition

Polycrystalline silicon films were deposited at 800°-840°C in the same reactor described in Section 3.4.1. Films were deposited from silane at 30 to 40 nm/min. Total thickness ranged from 0.12 to 0.6 micron. Dopant was not added to the gas stream, but these films were doped as in the epitaxy cases. Both (111) and (100), 0.003 ohm-cm, arsenic doped silicon was used for substrates. For most samples, the native oxide film was etched off the wafer prior to film deposition as for epitaxial deposits. This step was omitted in two cases for testing the effect of the oxide layer, although all wafers were cleaned in HF before loading the reactor at room temperature.

3.5.2 Composition

In Figure 25, the arsenic dopant concentration profile was measured by SIMS analysis before and after pulsing, and the carrier concentration was measured with a C-V profiler after pulse processing. The concentration scale was fitted to the substrate resistivity. The error bars are the noise limits from the SIMS analysis, 0-5 counts/second at low concentration and ± 5 counts/second at higher concentrations. The doped scale was fitted from crater measurements.

Differences between films deposited by CVD and LPCVD techniques can be seen in comparing Figures 25 and 21. Both as-deposited films show a sharp step in the dopant concentration profile at the film substrate interface. However, the width of the transition region for the 800^{o}C polysilicon CVD film is over 100nm compared to less than 25nm for the LPCVD film. After pulse epitaxy, with melt beyond this interface, both profiles are similar, and exponential. The sensitivity for arsenic in the data for Figure 21 was greater than that in Figure 25 due to changes in sputtering rate and sputtering ion.

The active carrier concentration in the regrown film, shown by the C-V profile, is lower than the arsenic concentration detected by SIMS. This might represent the actual dopant concentration, since the signal from the former analysis was so low, or it could represent compensating defects in regrown epitaxial layer caused by fast quenching. The discrepancy was not resolved.

3.5.3 Structure

Surface morphology of polycrystalline silicon films was sensitive to contaminants. Smooth, reflective films were always obtained on substrates whose surfaces were not etched in situ. However, the film growth at low temperatures on etched substrates was sometimes grainy (under an optical microscope) and nonreflective. In addition, these films often showed "tweezer marks" where contaminants from handling affected film growth.

An SEM photomicrograph of the surface structure on such films is shown in Figure 26. Raised pyramid structures about 0.5 micron high, often partially distorted as shown, covered the as-deposited surface and changed the optical properties. These structures were melted smooth by pulsed electron beam irradiation. Another change by PEBA in surface morphology is the disappearance of the cellular structure after pulsing, seen prior to pulsing in Figure 26.

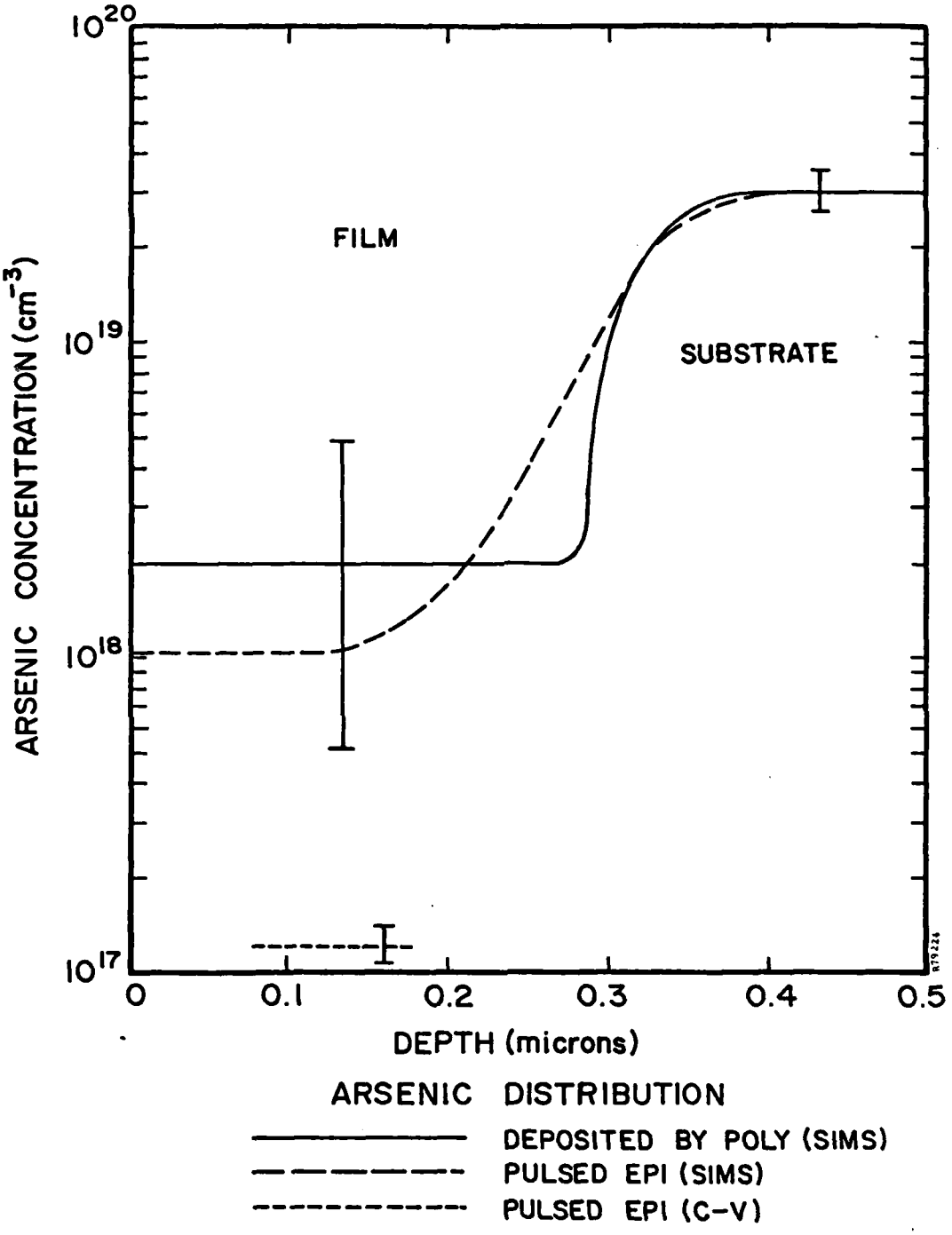

Figure 25. Dopant profiles in as-deposited poly films and after pulsed electron beam epitaxy.

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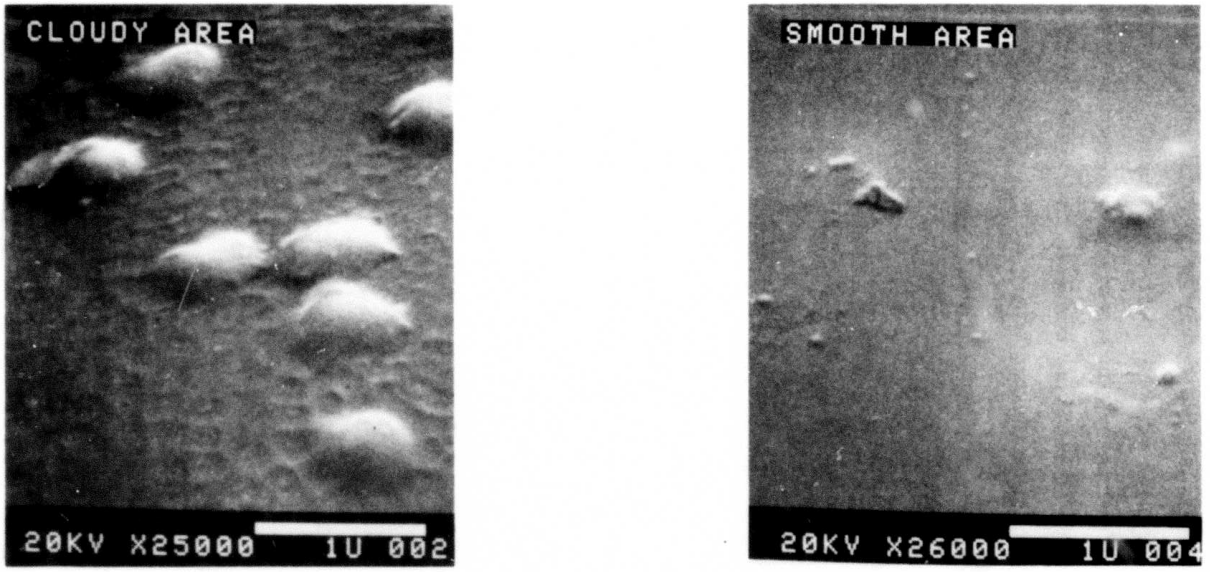

SEMS (x25,000) OF 3000 Å, 800°C CVD POLY-Si
BEFORE AND AFTER PULSE ELECTRON BEAM RECRYSTALLIZATION

Figure 26. SEM images at 25,000x of 0.3 micron, 800° CVD polysilicon film at low and high PEBLE fluence showing how spikes are removed by melting.

The polycrystalline films were also analyzed by electron channeling and RHEED. The fine, randomly oriented grain structure seen in LPCVD films was not observed. All of the polysilicon films deposited at high temperature (over 800°C) showed strong orientation to the substrate. Electron channeling patterns could not distinguish between the polyfilms and epitaxial films. Typical RHEED patterns showed badly twinned, single-crystal films were deposited rather than true polycrystalline silicon with randomly oriented grain structure. After pulsing, these films converted to epitaxial films with strong Kikuchi lines.

Although this analysis suggests that the polysilicon deposits were very close to the parameters for epitaxial deposition of silicon films from silane, these films had many defects and were not suited for making devices.

3.6 DEVICE IN PULSED EPITAXIAL FILMS

Schottky barrier diodes were fabricated on pulsed epitaxial films. The substrates were 0.07 ohm-cm antimony doped silicon with 0.4 micron LPCVD polyfilm deposited without etching the oxide in situ. The diodes were 5.71 mils in diameter and of an alloy (0.7 Ni, 0.3 Cr) with a gold overlay for contacts.[38] The typical diode I-V curve is shown in Figure 27. It is a functional, but leaky device. A C-V profile was measured; I/C^2 versus V is plotted in Figure 28. The intercept at C=0, about 0.2 volt, is low for the expected barrier height. Diodes were fashioned on a comparison sample, a 0.2 micron CVD epitaxial layer on the same substrate; however, they were nonfunctional. This leaves the question unanswered whether the less than ideal diode characteristics in Figures 27 and 28 are due to the material or due to the contacts.

3.7 SUMMARY

It has been shown that PEBA can convert deposited silicon films to epitaxial layers on single crystal substrates. The results are sensitive to the thickness of the deposited layers, the structure of these layers, and the thickness of the oxide at the interface. Functional devices have been fabricated in this material.

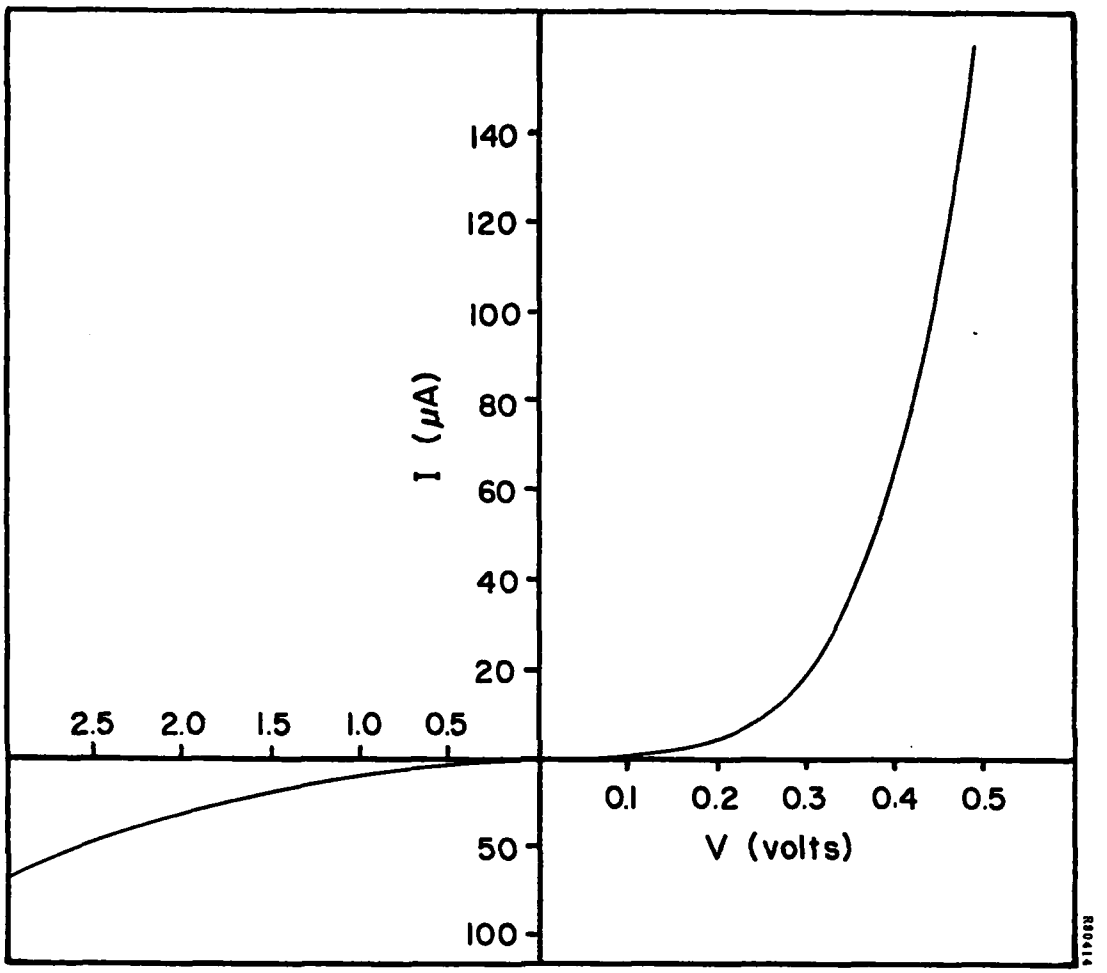

Figure 27. Current-voltage characteristics for Schottky barrier diodes on pulsed electron beam recrystallized material (0.4 micron thick, nn^+).

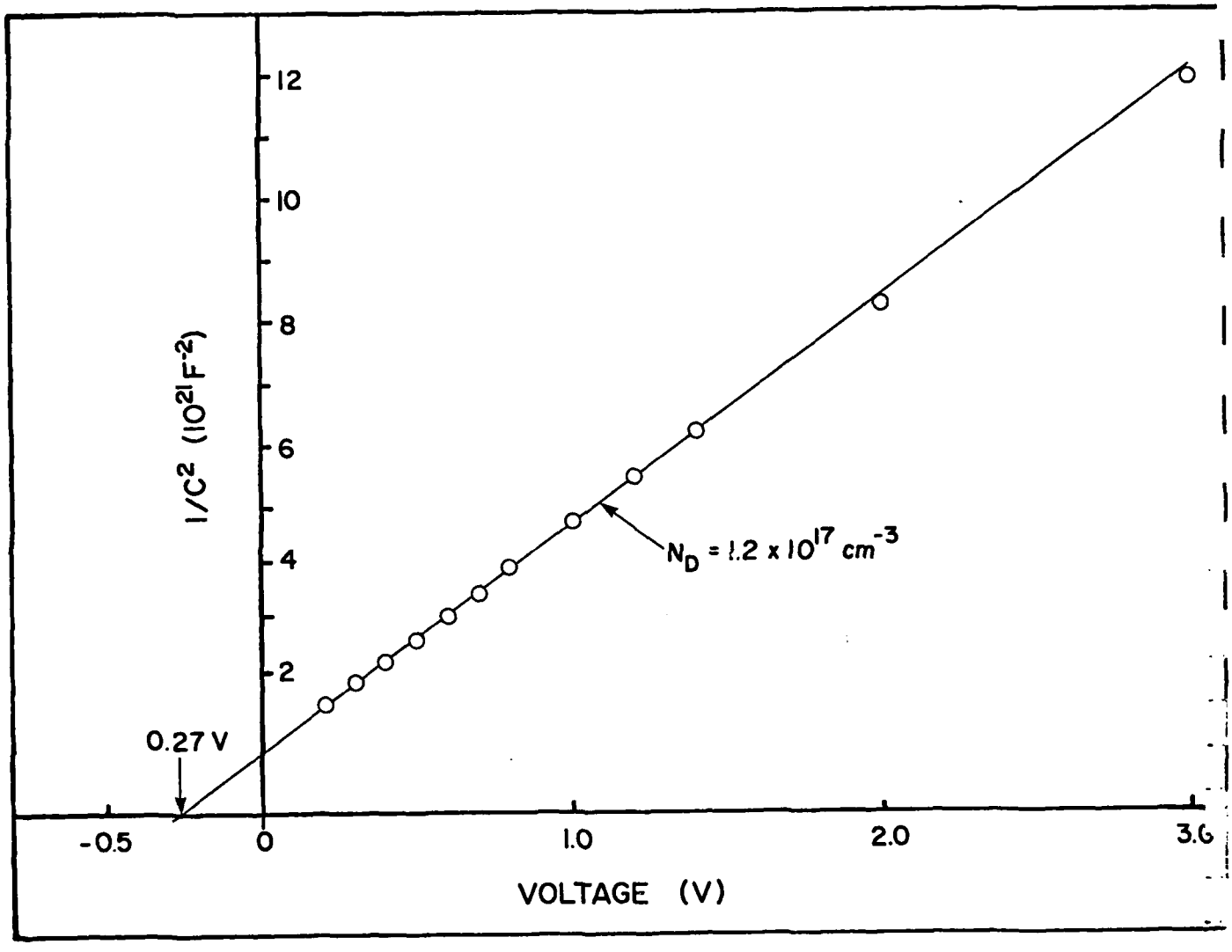

Figure 28. Capacitance-voltage characteristics for 145 micron diameter Schottky barrier diodes on pulsed electron beam recrystallized material (0.4 micron thick, nn^+).

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